SUPPLY - FRIENDLY

SINGLE PHASE

UNINTERRUPTIBLE POWER SUPPLY

CJ Mills

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UNINTERRUPTIBLE POWER SUPPLY

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Terms of Reference

Uninterruptible power supplies (UPS) are used to maintain a continuous supply of power to a critical load.

The project proposed by Mr. Michel Malengret was to design a microprocessor controlled UPS to meet the following specifications:

- The UPS must provide a 230V±1% single phase 50Hz output.
- The harmonic content of this output should be less than 5% of the fundamental.
- When the rated load is suddenly applied or removed, the inverter output shall not vary by more than 5%.
- Under normal operating conditions the UPS should drawn a current from the supply at almost unity power factor.
- Investigate the possibility of modifying an existing UPS system.
- The UPS should be equipped with an interface to facilitate remote monitoring.

Synopsis

Uninterruptible power supplies (UPS) maintain a constant supply of power to a critical load. The distinguishing features are a fixed voltage and frequency, low harmonic content and the ability to supply the load for a period of time after the incoming supply has failed.

The document begins by identifying the typical power-line disturbances and their effect on various types of equipment. Together with the power conditioners used to suppress these disturbances, various UPS standby, line-interactive and on-line configurations are introduced.

Next, the possibility of modifying a locally manufactured UPS to meet the design specifications is investigated. The performance of the system under load is evaluated and forms the basis for the following decision. Due to the large number of modifications required and the inflexibility of local UPS topology, an alternative topology is adopted.

In the new topology a power factor corrector, constructed around a DC to DC boost converter, interfaces with the incoming AC line. It delivers a half sinusoidal current into the DC bus. An IGBT inverter using sinusoidal unipolar pulse-width modulation regenerates the AC load voltage after filtering through a LC-filter. The DC bus voltage ripple is reduced by synchronising the inverter load and power factor corrector current while the battery pack maintains the DC bus during a power failure.

The power factor corrector employs a dedicated analogue controller chip while a MCS-51 microcontroller generates the inverter PWM, provides the remote monitoring facilities, battery charging and performs general support tasks.

The total harmonic distortion of the input current is measured at less than 4% while the power factor remained above 0.99 over the entire load range. The ripple regulator reduced the DC bus voltage ripple without any noticeable effect on the load. Under maximum load, the steady state output voltage is maintained during the -20%, +10% variation in the incoming line voltage. However, the transient response fails to meet the 5% design specification. A 0-100% load step results in a 7% drop in the output voltage while the loss of the load results 10% jump in voltage. System efficiency is measured at 85%.

It is the lack of processing power, precluding the use of floating point or an optimal control algorithm, which ultimately compromises the performance of the system.

It is recommended that the microcontroller be replaced with a 16-bit processor or digital signal processor to provide the extra computational power needed to optimise the UPS response. To improve the voltage regulation, it is recommended that the control include an inner current loop while the switching frequency should be increased to reduce the energy storage in the output filter. Further adjustments and refinements to the topology are suggested in the final chapter.

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1. Introduction

An uninterruptible power supply (UPS) provides a continuous flow of *quality* power to a critical load, independent of the condition of the primary supply. Quality power refers to steady state voltage regulation and transient regulation as well as the harmonic content of the output waveform. The performance characteristics that distinguish a UPS from other static AC power supplies are:

- A constant voltage and frequency output while the primary supply fluctuates.
- Low harmonic content.
- Fast transient response time.
- The ability to supply the critical load power for a period of time after the primary supply has failed.

The need for the UPS has grown dramatically over the last decade. This growth in the market has been fuelled by the increased use of electronic equipment such as personal computers, network stations and AC drive controllers. The proliferation of electronic equipment has resulted in the '*pollution*' of the AC mains in the form of unwanted harmonics. These harmonics are generated by the switching currents used in the power supplies and inverter drives. The increased number of consumers connected to the local power grid, combined with the problems associated with harmonic injection (reactive currents, losses etc.) have reduced the ability of the local grid to supply quality power to its users. This has meant more frequent line sags, over-voltages, spikes and power failures.

The effect of powerline disturbances on the sensitive equipment depends on the type of equipment, whether any power conditioning equipped is installed and on the form and magnitude of the disturbance.

Sustained under-voltages may cause motor drive controllers to trip out, which is highly undesirable in certain applications e.g. paper-mill. Over-voltages are known to fuse light bulbs and damage television tubes.

Large repetitive voltage spikes can destroy electronic equipment. During a thunder storm, a single lightning strike can discharge over 400 billion watts within a 50 to 500 microsecond duration, easily inducing thousands of volts in nearby powerlines. In laboratory tests[1], it has been shown that a repetitive energy level of $^1/_{1000000}$ joules is capable of destroying a PN junction buried within a microprocessor. With an average storm consisting of a number strikes per minute, the risk to sensitive equipment is substantial.

The effect of a total loss of power depends on the duration of the failure and the equipment design. A personal computer (PC) power supply is designed to maintain its output for a maximum of 2 cycles ($\approx$100 milliseconds). Thereafter a logic signal from

[1] Bedford, M.; "Stormy Weather - Lightning Protection", Computer Shopper, pp. 501-508, January 1995

the supply allows the computer an additional 50 milliseconds within which to backup any information. Unfortunately, the configuration of PC's (harddisks, memory etc.) vary and with it, the power supply hold up time. Generally, unless the supply returns within a couple of milliseconds, the user will lose all the information. To combat the reduction of power quality, the resultant loss of production and associated costs, many users are now powering their sensitive loads through a UPS.

This report details the design of a UPS capable of supplying quality power to these and other sensitive electronic loads. The objectives are:

- To design a supply friendly on-line single phase UPS.
- To ensure that the total harmonic distortion of the output is less than five percent.
- To ensure the output voltage is maintained within five percent when the rated load is suddenly applied or removed.
- To equip the UPS with a remote monitoring facility.

The report is developed as follows:

- In the first section, the typical powerline disturbances are introduced. Various power conditioners and UPS topologies are also described.
- The performance of an available standby UPS is analysed.
- A new topology is developed using information gleaned from the above analysis and a literature survey.
- The design of the power electronic components is detailed.
- The design of the digital controller is covered including the control algorithms.
- The new topology is assembled, debugged and its performance analysed.
- Finally, alterations and improvements to the topology and controller are proposed.

2. Improving Power Quality

In this section, the typical powerline disturbances are described and how power conditioners are used to protect sensitive equipment. Finally, uninterruptible power supplies and their various topologies are introduced.

2.1 Typical power-line disturbances

A total loss of power is generally caused by severe weather conditions. A direct lightning strike may require the opening of breakers to protect equipment on the distribution grid.

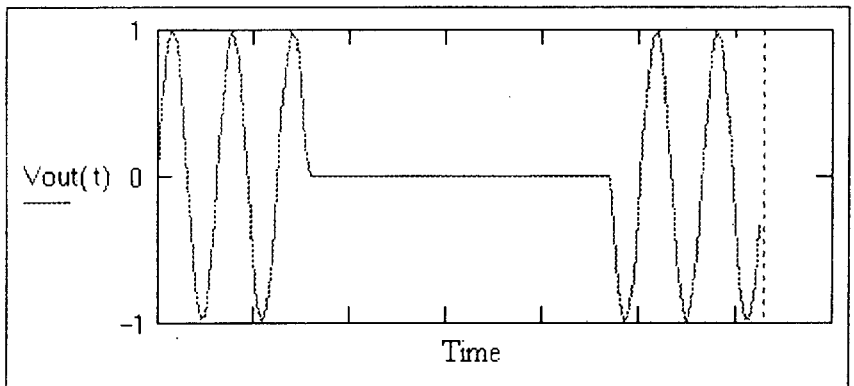

Figure 1: Supply line failure

High winds sometimes dislodge trees which fall and break nearby power-lines while flooding can short-circuit underground cabling, resulting in outages lasting an hour or more. Other factors contributing to a loss of power are transformer and generator failures. Under these circumstances, a couple of minutes may pass before the circuit breakers redirect the load onto an alternative supply. The cost of such an interruption for users can only be estimated. For an automotive assembly line its R920,000 while for a semiconductor manufacturer its around R80,600 to R3,680,000. At a probability of 0.001 for a 15-minute interruption, computer users loose around R130,300,000 per year.

Although a voltage sag lacks the severity of a power failure, it does nonetheless inflict

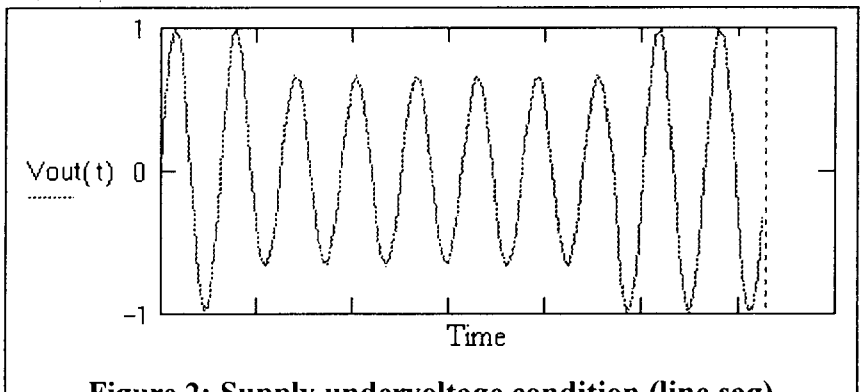

Figure 2: Supply undervoltage condition (line sag)

a certain measure of damage to a number of users. A voltage sag of just 250 milliseconds can trip a paper manufacturing machine, resulting in hours of downtime and possible equipment damage. In the synthetic fibre industry, a voltage sag of 50 milliseconds can shut down spinners, entailing long costly cleanups, product waste and lost production. Voltage sags are result of overload conditions or the turning on of heavy equipment such as furnaces and large induction motors.

An over-voltage condition is caused by a sudden decrease in the system load or by incorrect transformer-tap settings at a substation. A sustained over-voltage may cause some equipment to trip out while destroying others.

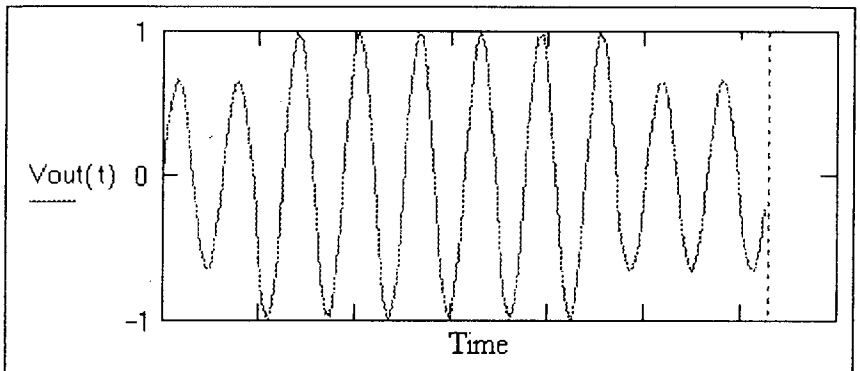

Figure 3: Supply over-voltage condition (line swell)

Harmonic distortion, usually low-order multiples of the line frequency, are the result of converters and inverters connected onto the same circuit.

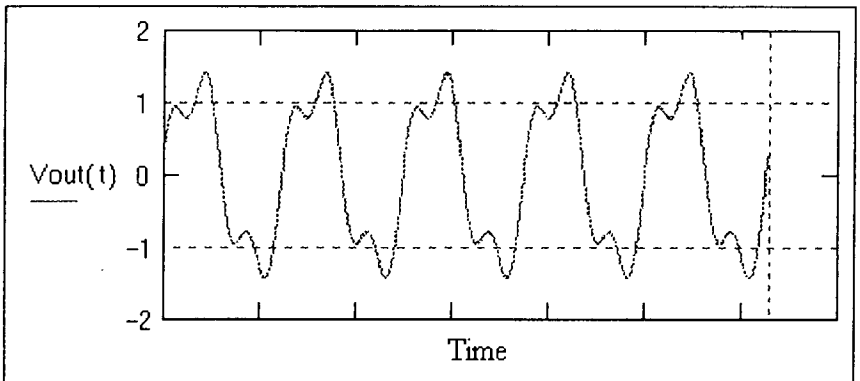

Figure 4: Harmonic distortion of the supply

The harmonics generally exist on a sustained basis, influencing the operation of some equipment. For example, mains signalling is a method by which signals can be superimposed on the mains wiring for the remote control of electrical equipment. If the harmonics injected correlate with the remote control signals, mains-signalling equipment will cease to operate reliably.

Another form of waveform distortion, besides harmonic injection, is commutation notches.

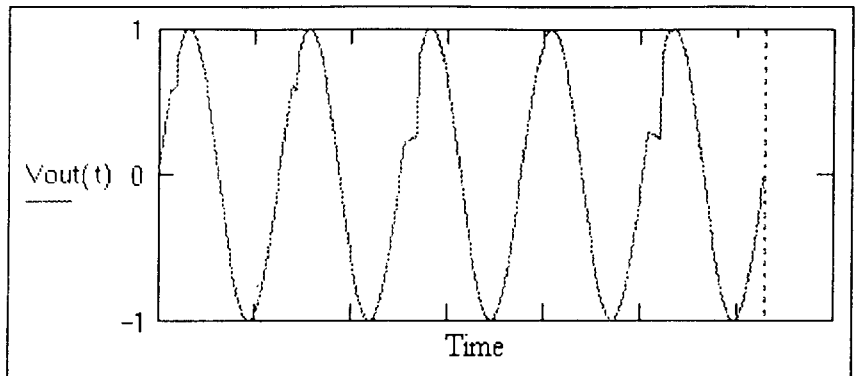

Figure 5: The effect of commutation on supply

This is the result of circuit breaker closings, powerline feeder switching and other short circuits caused by power electronic equipment such as AC to DC thyristor converters.

Although frequency deviations are not a major problem for an interconnected AC power system, they are the result of region-wide network problems such as the loss of a primary feeder or generator instabilities.

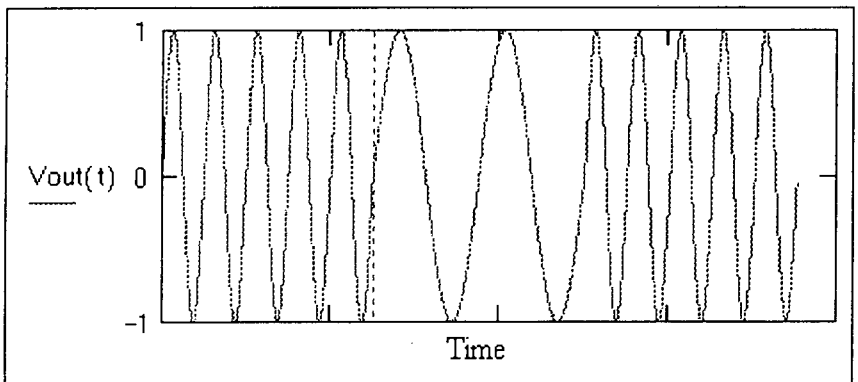

Figure 6: Supply frequency deviation

High frequency noise (EMI) is generated by most power electronic equipment due to the rapid switching of voltages and currents. It is also generated by air-conditioners, the arcing of welders, furnaces and thermostats.

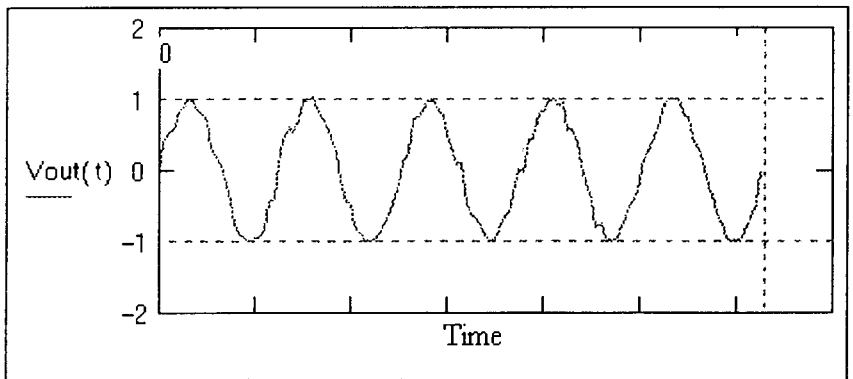

Figure 7: Noise on the supply

Supply line surges or spikes are probably the most dangerous disturbances since they generally inflict the most damage. They are the result of lightning strikes, system faults, powerline feeder switching, power factor capacitor switching and sudden load changes.

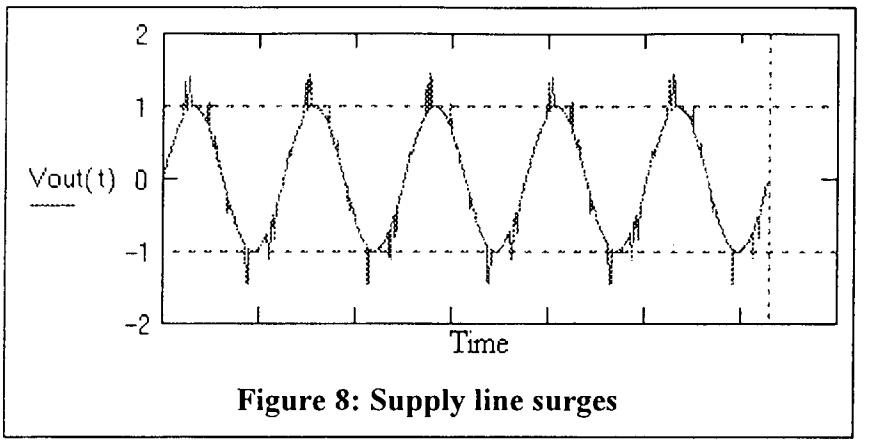

Figure 8: Supply line surges

In the figure below, the voltage level and occurrence for a lightning induced spike is given for three typical environments: an office environment, a light industrial zone and a rural site. The figure clearly shows that within the office environment, electronic equipment should expect a number of spikes to exceed 3000 volts.

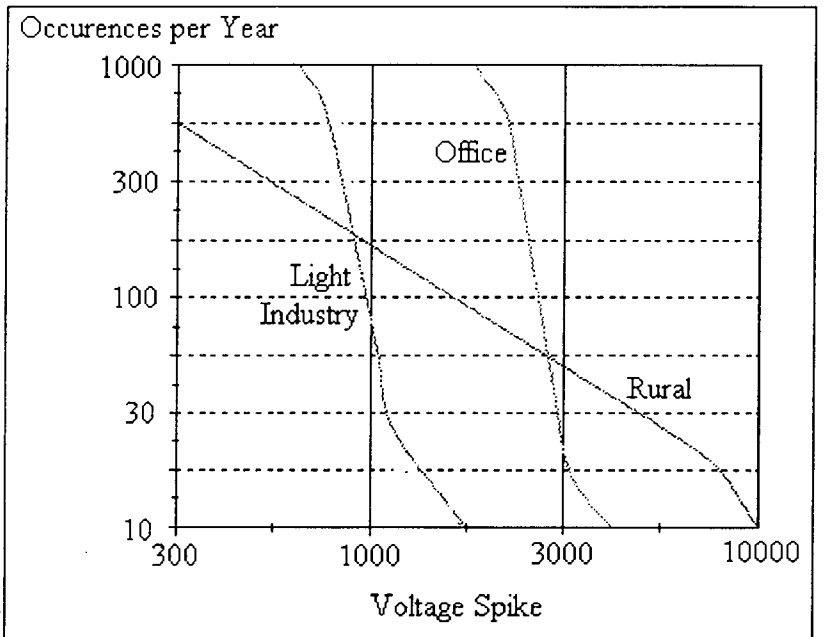

Figure 9: Likelihood of a lightning induced voltage spike

2.2 Power conditioners

Power conditioners provide an economical and cost effective means of suppressing most of the typical powerline disturbances. The basic configurations include shunt and series surge suppressers, line filters, isolation and Ferro-resonant transformers.

2.2.1 Surge Suppressers

Surge suppressers do not eliminate the voltage spike but rather ensure that it remains within certain boundaries. The designs are based on a shunt or series configuration. The most common device used in shunt suppressers is the metal oxide varistor (MOV).

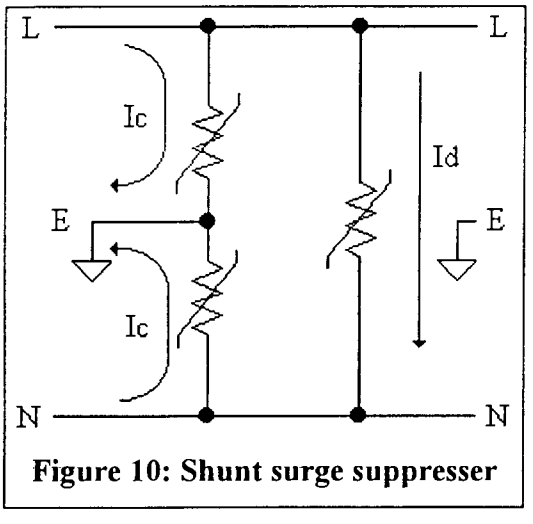

Figure 10: Shunt surge suppresser

At a low voltage, the device appears as a capacitor to the connected circuit. As the voltage increases, this effect disappears and the device acts as a voltage dependent resistor. Throughout its normal operating range, it conducts only a couple of milliamps. When the voltage stress across the device is large (spike), breakdown occurs and a much larger current (≈amps) flows. The duration and magnitude of this current impulse is used to calculate the required energy rating for the MOV's. The devices are usually oversized so as to prolong their life expectancy i.e. number of operations.

The basic shunt surge suppresser consists of a MOV connected across the supply terminals to suppress differential-mode voltage spikes I_d. Two additional MOV's, connected from each supply terminal to the earth return line, are required to suppress common-mode voltage spikes I_c. It should be noted that the MOV has no effect on spikes or surges below the threshold voltage. The MOV also has a clamping response time which implies that spikes of very short duration are unaffected.

Functionally, series surge suppressers act as a series impedance which varies from a low resistance under normal operating conditions to a high resistance when the transient appears. Two distinct advantages of using a shunt versus series suppresser are the absence of insertion loss and the simplicity of the circuit arrangement. However, since a shunt suppresser presents a low impedance to the transient, it must be able to absorb large amounts of power under pulsed conditions. The most practical method of surge suppression is a combination of series and shunt networks.

2.2.2 Line Filters

The line or EMI filter is a passive bi-directional low pass filter with a roll-off at the line frequency. The filter prevents mains-borne disturbances from interfering with the operation of the equipment while also preventing the equipment from conducting high-frequency noise back into the utility grid. Capacitors alone cannot secure the required fall-off for the filter. The attenuation is improved by using one or more chokes. In general, the choke with the highest inductance is the most effective. However, the voltage drop across the choke rises with inductance, therefore the value must be chosen based on the load and the anticipated interference. Most EMI filters are based on a π-configuration with a current-compensated toroidal choke. In this configuration, the inductance of both chokes is low while ensuring a small voltage drop at the expected load current.

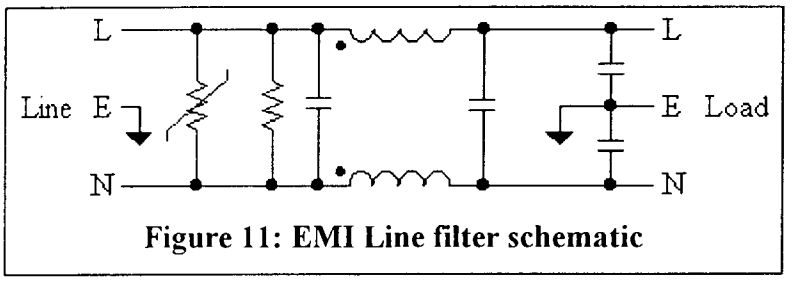

Figure 11: EMI Line filter schematic

The capacitor values are a carefully established compromise between acceptable switch-on and switch-off currents and the risk of electrical shock in the case of defective or improperly connected earthing. Although the filter reduces mains or equipment generated interference, a spike or surge may excite the system and lead to resonance. For this reason, the filter is usually combined with a surge suppresser (MOV etc.) to quench possible oscillations.

2.2.3 Isolation Transformers

An isolation transformer with electrostatic shields not only provides galvanic isolation but, due to the primary inductance, also filters the differential and common-mode voltage spikes.

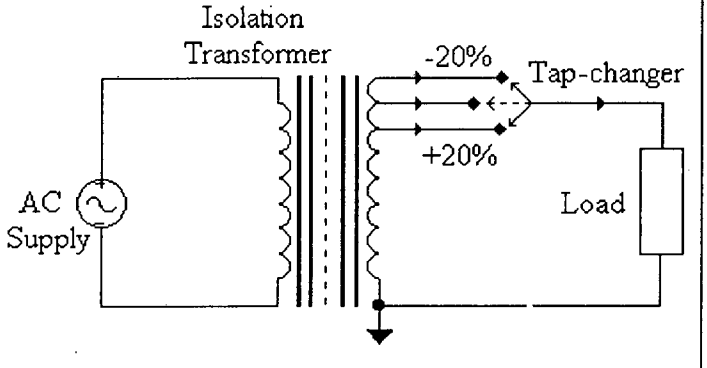

Figure 12: Isolation transformer with a tap-changer

Compensation for voltage sags and over-voltage conditions may be achieved by the addition of a tap-changer. The number of secondary winding tap points determines the precision with which the output voltage can be controlled. The taps are usually placed so as to compensate for a ±20% variation in the input voltage.

2.2.4 Ferro-resonant Transformers

If an ordinary transformer operates at a high enough primary current, its core will saturate. Increasing the primary current any further will then not increase the secondary voltage. Consequently, operating an ordinary power transformer in saturation will create a *voltage regulator*, though such operation is impractical since the primary saturation current is close to a short circuit.

The Ferro-resonant transformer, on the other hand, is designed to operate in saturation. Since the secondary coil operates in saturation and not the primary, more flux must be produced in the secondary leg than in the primary. This is achieved by loosening the coupling between the windings with a magnetic shunt (air gap).

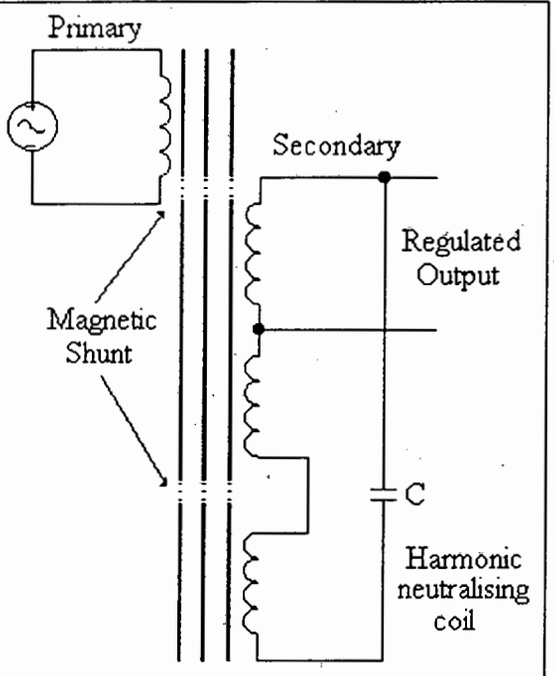

Figure 13: Ferro-resonant transformer with a harmonic filter

The output waveform of a basic Ferro-resonant transformer is similar to square wave and suitable for many loads, but it does not satisfactorily provide power for computer installations and their electronic loads without the addition of a harmonic filter.

The advantage of a Ferro-resonant transformer is its ability to attenuate differential mode transients. Since the secondary winding operates in saturation, transients and spikes are clipped. Ideally, 120dB of common mode rejection[2] is available. The transformer will also maintain the output voltage to within ±2-3% for a input variation as much as ±20%. Another advantage is its overload characteristics. If the output is short circuited, the current increases by only 80%. A well designed Ferro-resonant transformer can maintain a short circuit indefinitely.

Unfortunately, the Ferro-resonant transformer is a tuned circuit and is thus frequency sensitive. Typically, a 1% (0.05Hz) change in frequency produces a 1.5% (≈5V) change in output voltage. Another drawback is its efficiency: usually 88-90%. The wasted energy is radiated from the transformer core as heat.

2 Michele, F.; "Stabilising the mains with ferro-resonant technology", E+W World, February 1992

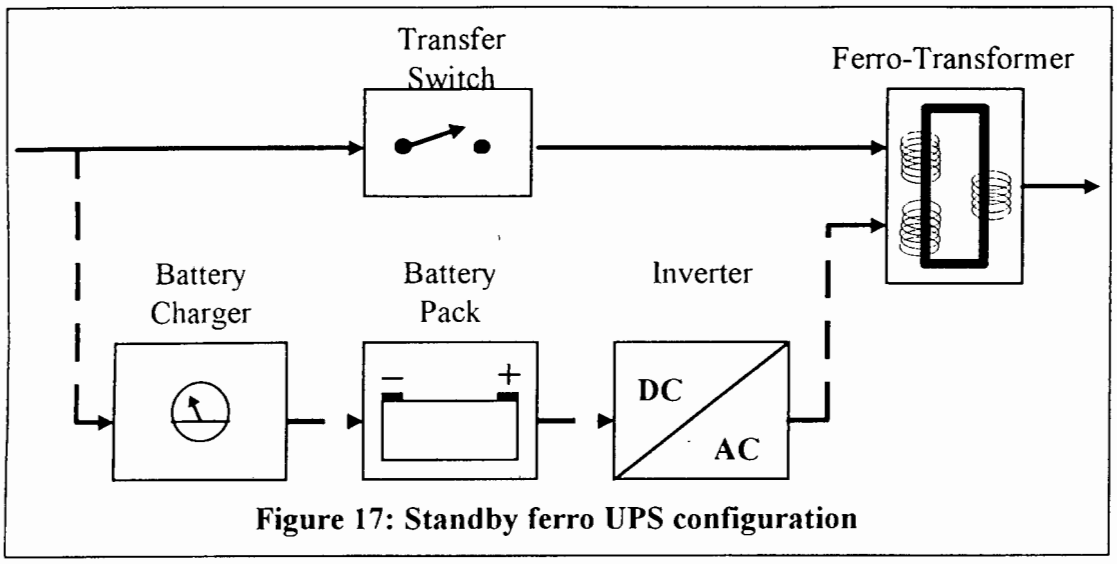

Figure 17: Standby ferro UPS configuration

The *line interactive* UPS powers the load directly through the inverter. The inverter is also used to regulate the load voltage and charge the battery when operated in reverse as a rectifier.

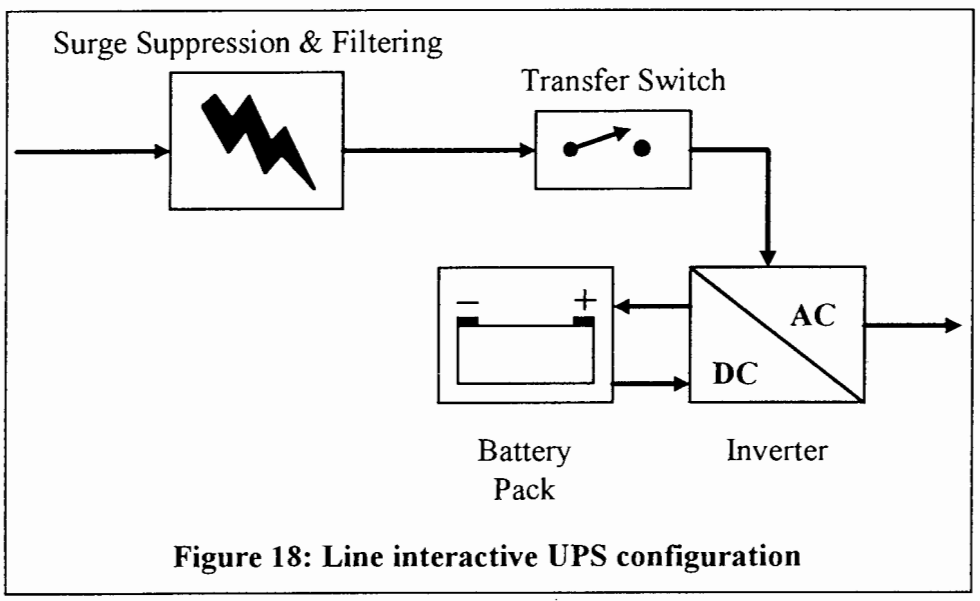

Figure 18: Line interactive UPS configuration

Uninterruptible power supplies, in their various configurations, provide this protection as well as the ability to maintain the load in the event of a total loss of supply.

In the next chapter, a standby-type UPS is analysed.

3. Standby UPS Analysis

In this chapter, a locally manufactured UPS is presented. The standby-type topology is detailed and its performance with various loads analysed.

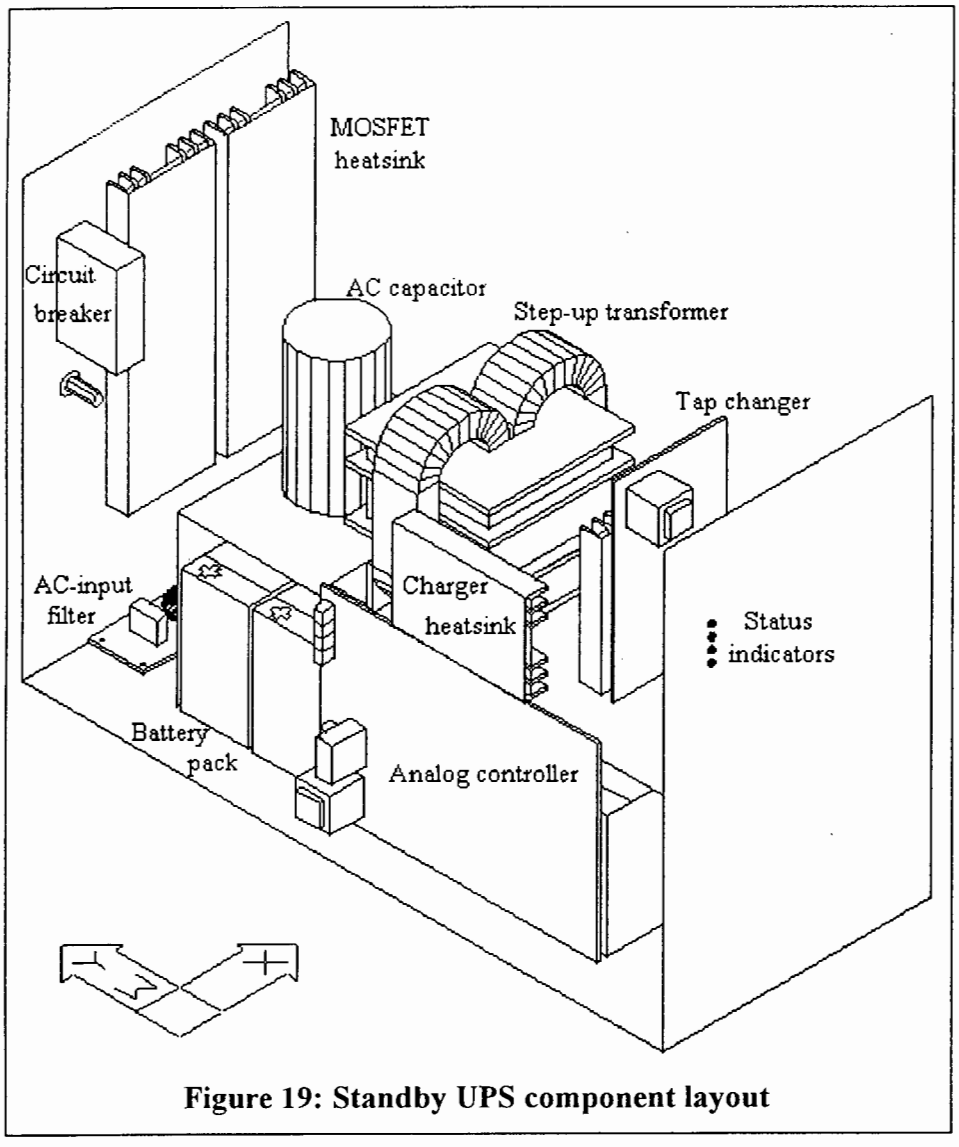

Figure 19: Standby UPS component layout

3.1 Overview of the Topology

Refer to Figure 20. Under normal operating conditions, the bypass switch is closed. This enables the tap-changer to compensate for primary supply voltage variations. During a voltage sag, the lower tap is selected in order to boost the output voltage. Over voltages are catered for by selecting a higher tap-point. The load however remains connected to the centre tap.

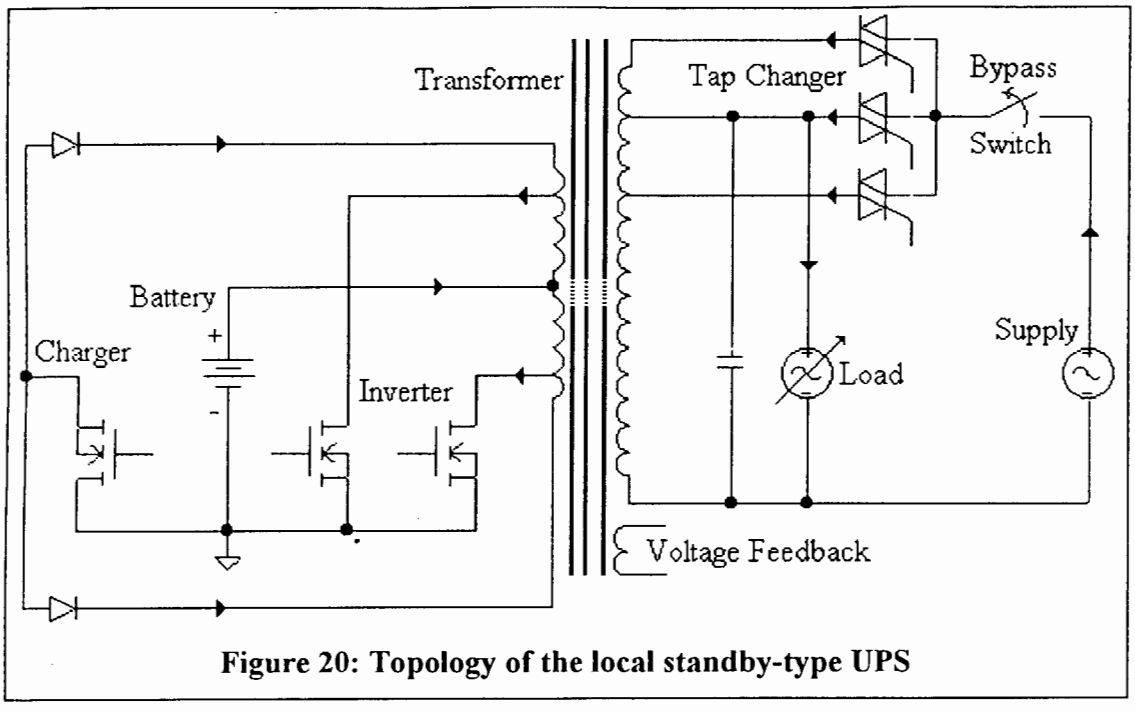

Figure 20: Topology of the local standby-type UPS

When the supply fails, the bypass switch is opened to prevent the UPS from injecting energy back into the supply. At the same time, the PWM inverter is enabled and begins to power the load from the battery pack. The inverter is arranged in a standard push-pull configuration. The main advantage of the push-pull circuit is that no more than one switch in series conducts at any instant in time. This is important when operating from a low DC voltage source, where the voltage drops would result in a significant reduction in efficiency. The switch drive circuitry is also simplified since both switches share a common ground.

When switching occurs, the current shifts from one half to the other half of the primary winding. This requires very tight coupling to reduce the energy loss associated with the leakage inductance. It is also difficult to avoid the DC saturation of the transformer in a push-pull inverter due to the slight conduction imbalances between the switching elements.

One method of avoiding saturation is to break the DC path with a series connected capacitor. Under conditions where the output is unbalanced (i.e. a change in load effects only one half-cycle), the blocking capacitor develops a DC bias causing alternate cycles to be of different amplitudes. This introduces an unwanted sub-harmonic ripple into the output. An alternative method involves monitoring the average current and adjusting the conduction angles of individual switches. Unfortunately, extra harmonics are then introduced into the output waveform because of the asymmetric PWM. The current UPS system avoids saturation by introducing an air-gap into the core[3]. With an air-gap, the AC flux density ΔB_{AC} remains unchanged but the DC flux density B_{DC}, generated by the DC current component in the windings, is reduced to prevent saturation.

Although the sinusoidal PWM is filtered by the transformer, additional filtering is still required to reduce the harmonic content of the output to within acceptable limits. The

[3] Billings,KH.; "Switchmode Power Supply Handbook", McGraw-Hill, pg. 3-116, 1st Ed., 1989

filter is formed by connecting a capacitor in parallel with the output winding. The primary inductance, together with the series inductance of the air-gap combine to form a bandpass filter. During commissioning, the filter resonant frequency ω_o is tuned to the output frequency by adjusting the air-gap. The system is tuned until the output voltage is maximised i.e. $\omega C - {}^{1}/_{\omega}(L_{pri}+L_{air})=0$ and the admittance is a pure conductance at ω_o.

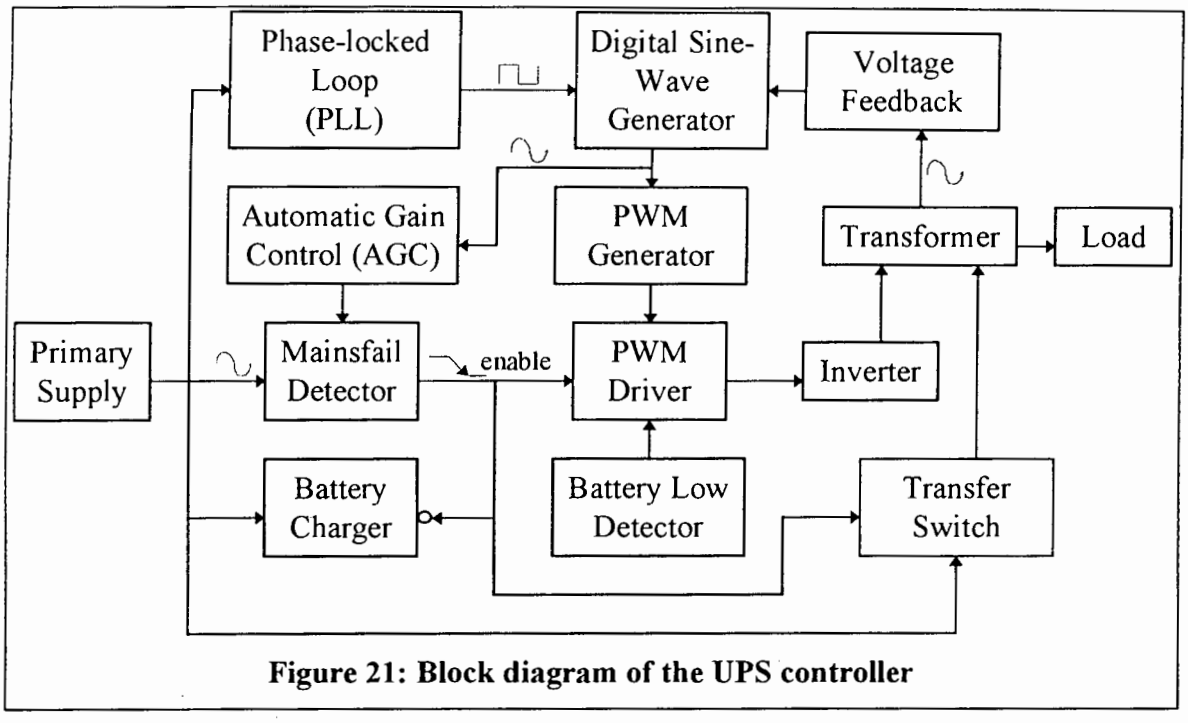

Figure 21: Block diagram of the UPS controller

An additional benefit of introducing the air-gap is the increased energy storage capability of the core. An air-gap decreases the slope of the *B/H* characteristic but does not change the required ΔB_{AC}. Hence there is an increase in the magnetising current ΔH_{AC}. This corresponds to an effective reduction in core permeability. However, the energy stored is inversely proportional to core permeability μ_{eff}.

$$Energy \alpha \frac{B^2}{\mu_{eff}} \qquad ...(1)$$

The energy is used to supply the load current during a primary supply failure and subsequent transfer to the battery backup supply.

The output is controlled by monitoring the voltage on a separate winding. This arrangement improves the UPS response by limiting the amount of switching noise fed back into the control system.

When the primary supply returns, the phase-locked loop (PLL) is enabled. Once locked onto the primary supply, the bypass switch is enabled and the PWM drivers disabled. At this point, the battery charger begins to recharge the battery pack. Depending on the depth of the discharge, the battery voltage returns to its float level within a couple of hours.

3.2 Performance analysis of the UPS

The output of the UPS (Figure 22), with a small resistive load applied, was digitised by a HP54600A oscilloscope and uploaded to a PC using ScopeLink V2.02. A Fourier transform performed on the 2000-point sequence using the Goertzel Algorithm[4] revealed a total harmonic distortion (THD) of 4.3%.

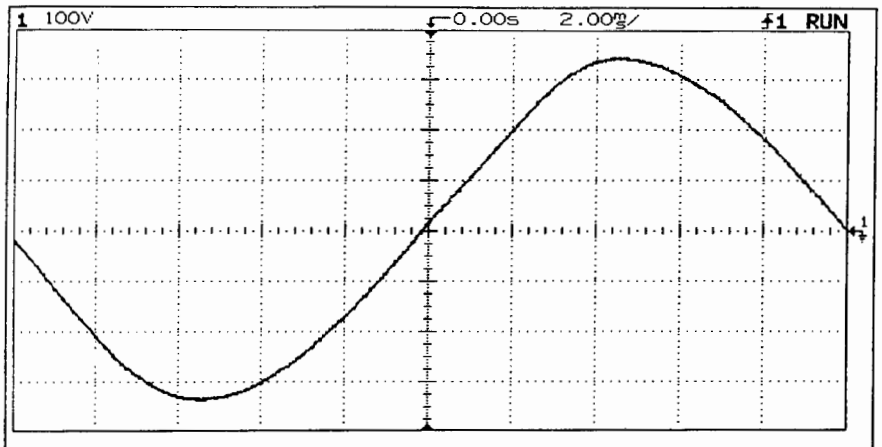

Figure 22: The local UPS output (lightly loaded)

In an attempt to distort the primary supply, three computers[5] were powered from the same outlet. The first trace reveals the poor condition of the primary supply. The second trace is the UPS output. As evidenced, the UPS does little to improve the waveform quality. Although the primary supply level of 223Vrms is close to the desired 230Vrms, the tap changer selected the lower tap, thereby driving the output to 255Vrms. Assuming the UPS was to provide emergency lighting, this output level would reduce the average lifetime of incandescent light bulbs by 8%[6]. This results in a net lighting cost increase of 30% per year.

[4] Brown, A.; "Goertzel alternative to the Fourier transform", E+W World, pp. 485-487, June 1993. Another algorithm which can be applied to a data set where N is not a power of two is the Winograd Fourier Transform Algorithm. Refer to Press, WH.;Teukolsky, SA. et al; "Numerical Recipes in C", Second Edition, pg. 509, Cambridge University Press, 1992

[5] Configuration: 486DX40+ 8M RAM+SVGA+340M Harddrive+Novell network

[6] Based on 230V/60W 1000hr incadescent lamp. See "Electronic energy-saving lamps with E27 screw or B22d bayonet bases", OSRAM

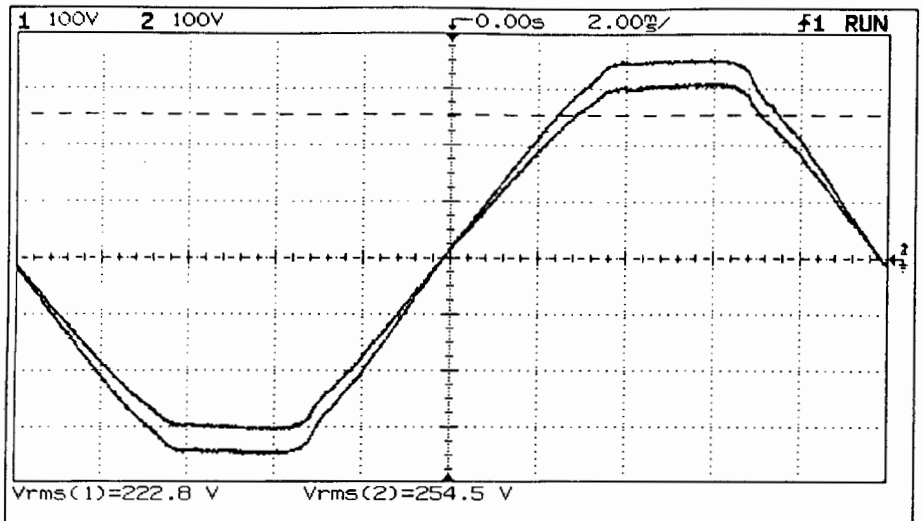

Figure 23: Primary supply versus the local UPS output

The load transfer response during a primary supply failure was simulated by connecting the UPS to the primary supply through a double-pole double-throw (*DPDT*) relay. The activation signal (*trace #1*) for the relay was then used to trigger the digital oscilloscope.

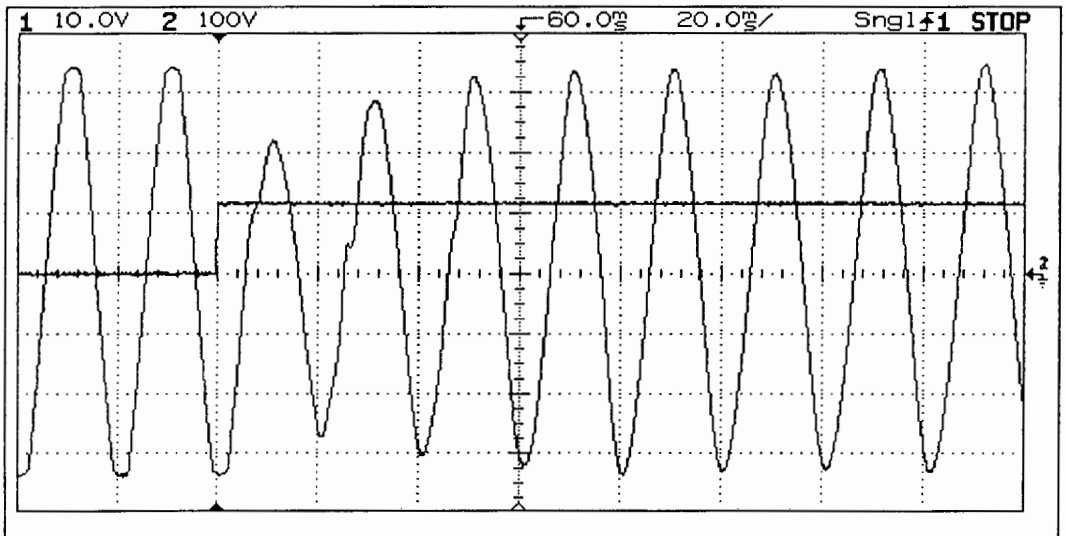

Figure 24: Transfer response with a 200W load applied.

For a 200W load, the peak output voltage drops by ≈100V. The transfer takes around 60 milliseconds before the voltage peak is within 5% of its final value, while the output voltage envelope oscillates for an additional 4-cycles before stabilising. However, for the same 200W load the following response was also captured. Refer to Figure 25.

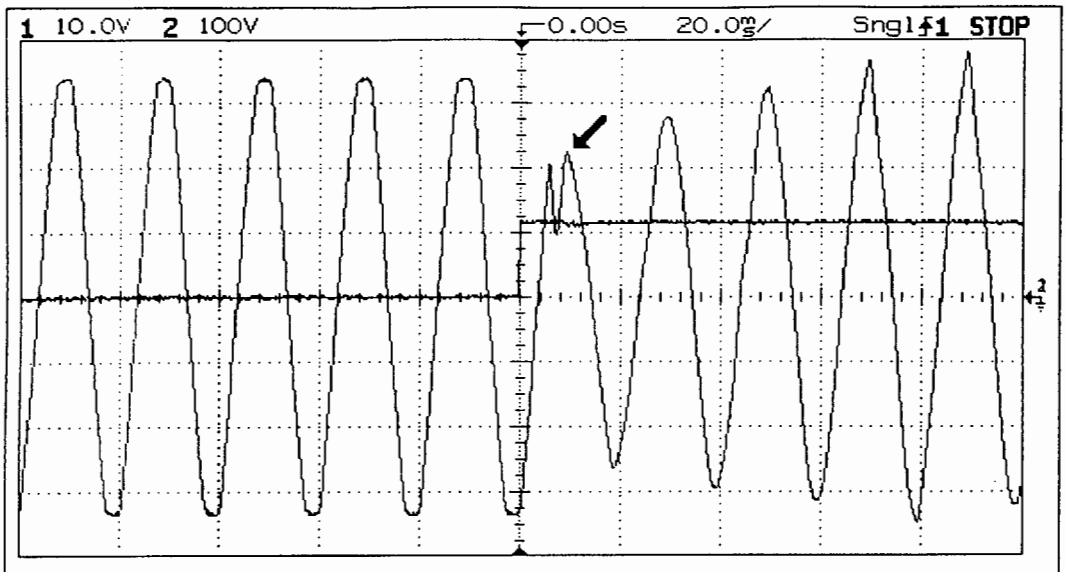

Figure 25: Transfer response with a 200W load applied.

Under close examination, the UPS yielded similar results for the 400W load (Figure 26).

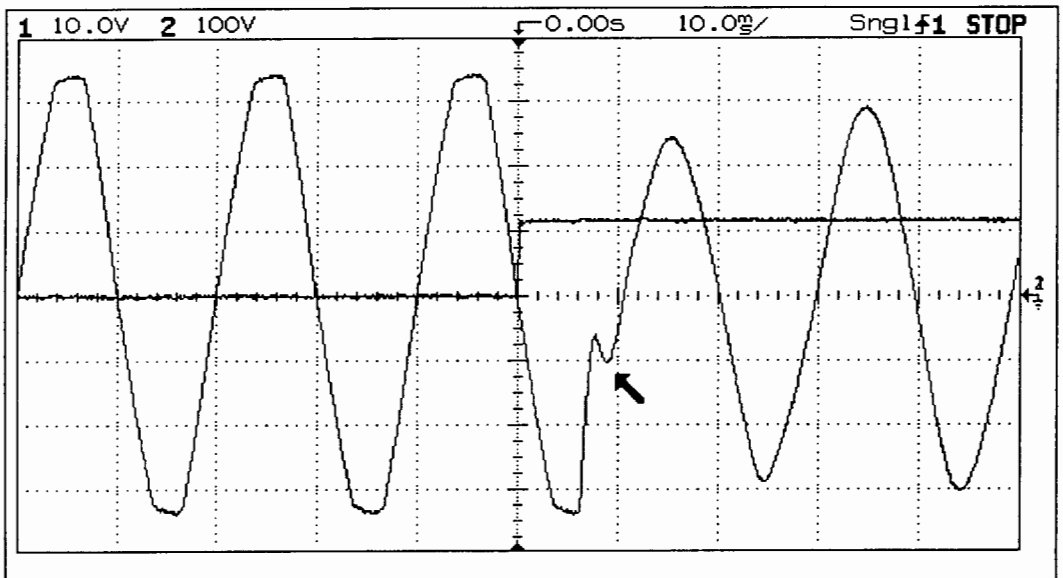

Figure 26: Transfer response with a 400W load applied.

The glitch as indicated in the above load transfers is caused by the slow response of the mains-fail detector. This is explained as follows: due to the mechanical nature of the test relay, the contactors open 6 milliseconds after receiving the rising edge of the activation signal. *The UPS must now detect this as the point of primary supply failure.* Meanwhile, the energy stored in the resonant circuit, formed by the transformer inductance and output capacitor, decays while supplying the load current (*and any other loads connected to the same primary supply circuit*). After a certain time, the UPS detects this failure. Only then does the PWM inverter begin operating and the bypass relay open to prevent back-feed into the primary supply. If the output voltage magnitude is increasing, the glitch is always generated since the resonant circuit cannot maintain the rise of voltage. However, if at the point of failure, the output voltage

magnitude is decreasing, the energy stored in the resonant circuit will reduce the load voltage $^{-dV}/_{dt}$.

In Figure 27, the inverter is disabled to highlight the effect of the energy storage on the output waveform. At a lower output current, the load is maintained without a glitch for ≈5 milliseconds after the power failure. Compared to the previous figure, it is clear that the ability of the resonant circuit to prevent glitches is a function of the load current.

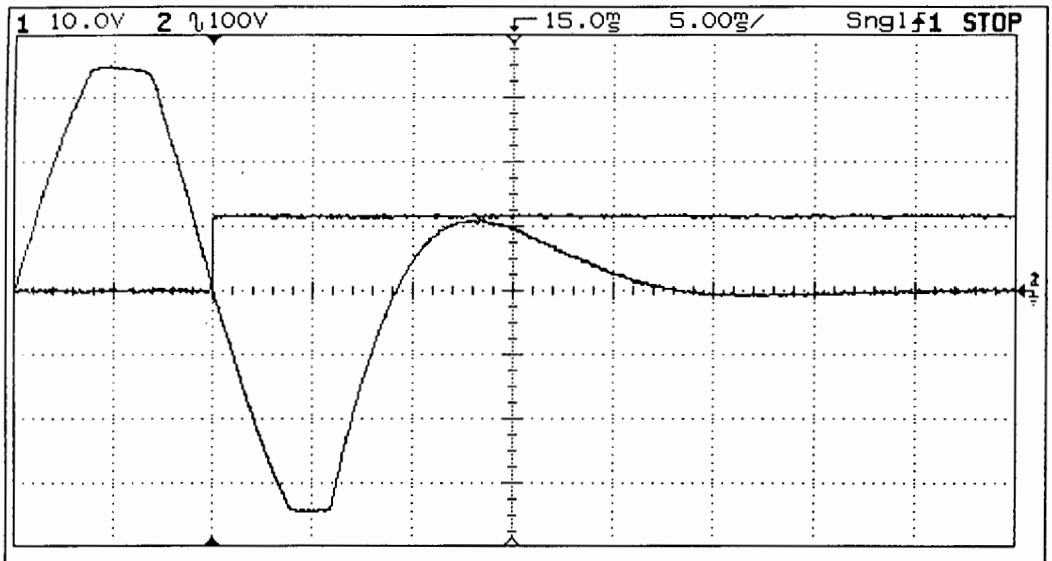

Figure 27: The effect of energy storage on the output waveform

In Figure 28, the efficiency of the UPS is plotted during a simulated supply failure. To obtain reliable and stable readings, a constant battery terminal voltage is required. Therefore, the battery pack was replaced with a high-current regulated DC supply. The load was then connected through a power meter.

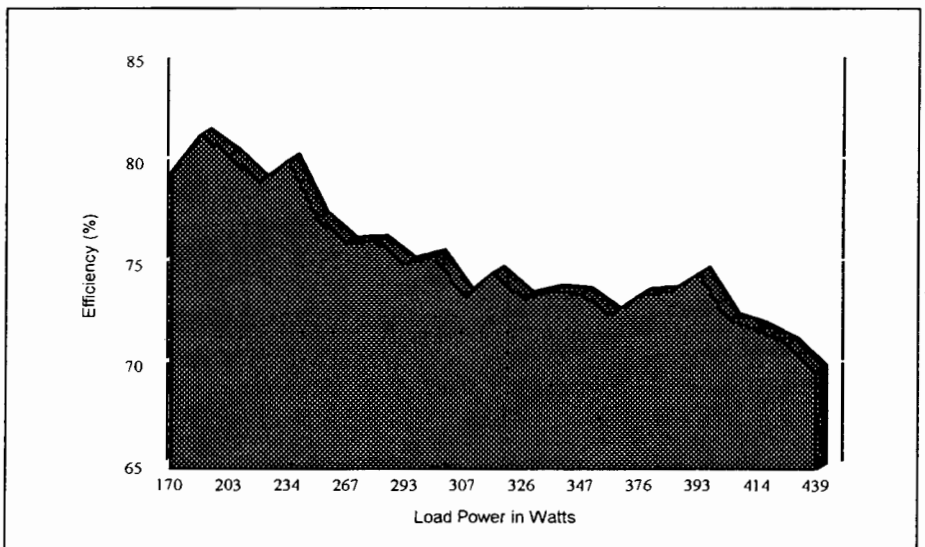

Figure 28: Efficiency versus Output Power (resistive load)

Under product specification, the manufacturer claims an efficiency of 80%, however resistive load tests reveal an average efficiency of 74%. At a load of 439 watts, efficiency has dropped to 70%. As the load approaches the maximum rated load of 500 watts, the efficiency plunges to just over 60% reducing the back-up time by almost 25%. Much of the wasted energy is dissipated as heat from the transformer, indicating its critical design. Fortunately, installed UPS systems are usually oversized to increase reliability and back-up time and therefore should never operate close to the maximum rated load.

In the following chapter, the development and operation of a new topology is described. Subsequent chapters will detail the design of the individual components.

4. Development of the Topology

In this chapter, the key issues of voltage regulation, harmonics and the supply failure transfer characteristic are addressed. Next a topology to satisfy the objectives is proposed. The chapters hereafter concentrate on the implementation of the various sub-sections.

4.1 Voltage regulation

To compensate for primary supply over and under-voltages, the locally manufactured UPS uses a tap-changer with an auto-transformer. This method regulates the output voltage in discrete steps e.g. V_{pri}-20%, V_{pri}, V_{pri}+20%. Continuous voltage regulation would require an infinite number of transformer taps. The following alternatives were considered: a shorting-coil regulator; an active power filter and a Ferro-resonant transformer.

4.1.1 Shorting-coil voltage regulator

Refer to Figure 29. The shorting-coil voltage regulator[7] is effectively a variable impedance controlled by a DC flux bias. Unlike conventional saturable reactors, it does not require an auxiliary DC source. The base drives of S1, S2 are synchronised with the primary supply and shifted with respect to each other by 180°. When the auxiliary coil on one of the limbs is short-circuited, the flux in that limb is '*frozen*' at the value when the switch is closed. The rate at which the frozen flux decays is determined by energy dissipated in the winding and switch element. Since the two switches are operated alternately, a DC flux component is established in the core. The magnitude of the DC flux depends on the triggering angle which in turn determines the point on the waveform at which the flux is frozen. Thus by varying the triggering angle, it is possible to obtain a DC bias without an auxiliary DC source. This method of establishing a DC flux ensures a continuous input current with a low harmonic content. Since the DC flux polarity and phase relationship of the input current with the supply voltage are controlled by the triggering angle, the regulator can operate at a leading or lagging power factor.

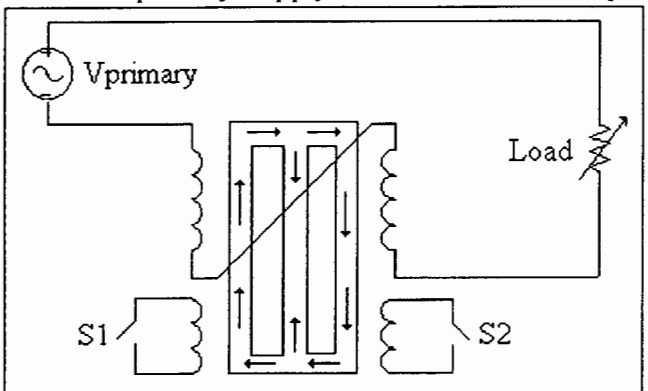

Figure 29: Shorting-coil voltage regulator

[7] Mehta, P.; Thomson, T.; Karim, AA.; "Shorting-coil regulator", IEE Proc., Vol. 128, Pt. B, No. 1, January 1981

In a UPS system, the shorting-coil voltage regulator can only compensate for overvoltages. Another disadvantage is an efficiency of only 80%. The wasted energy is dissipated in the auxiliary windings and switching devices.

4.1.2 An active power filter

Bhavaraju et al[8] proposed the active filter shown in Figure 30. A booster transformer is connected in series with the load. The load voltage is maintained by injecting a corrective voltage V_{inj} through the transformer secondary. To provide the ride through capability during a voltage sag, an AC chopper powered from an auxiliary source is employed on the primary side of the booster transformer. The AC chopper is controlled by a peak detector and PWM generator. Although the filter was shown to have a fast response (correction within a half cycle) and low harmonic injection, it does however require an auxiliary power supply. Bhavaraju et al suggested the use of a healthy phase as the extra supply, but this is difficult when only one (i.e. single) phase is available. The proposed filter only compensates for voltage sags - overvoltages could also be regulated if the AC chopper is replaced with a full bridge inverter.

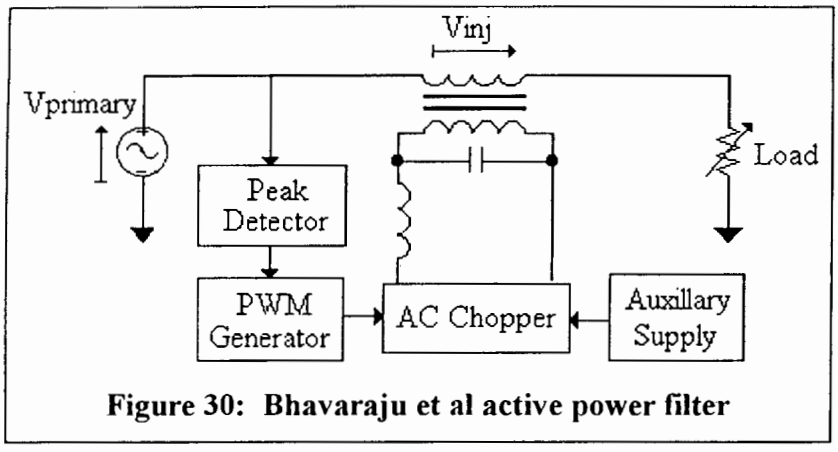

Figure 30: Bhavaraju et al active power filter

4.1.3 The ferro-resonant transformer

In the previous chapter, it was noted that because the ferro-resonant transformer is operated in saturation, it provides inherent voltage regulation. In a UPS system, a properly designed transformer could regulate the output voltage to within ±3% for an input variation of ±20%. Unfortunately, this does meet the 1% regulation objective. Another drawback of a ferro-transformer is its frequency sensitivity: typically a 1% change in line frequency produces a 1.5% change in output voltage. This attribute would interfere with the PLL as it minimises the phase difference between the input and output voltages.

4.2 Harmonic minimisation

The UPS objectives require that the THD of both the input and output be at most 5%. During an online resistive load test, the locally manufactured UPS achieved an output

[8] Bhavaraju, VB.; Enejeti, P.; "A Fast Active Power Filter to Correct Line Voltage Sags", IEEE TIE, Vol. 41, No. 3, June 1994

THD of only 4.3%. In standby mode however, a distorted primary supply voltage passed through the UPS with little reduction in harmonic content.

Usually a passive power filter and capacitor are used to attenuate the harmonics[9]. Unfortunately this approach has a number of disadvantages such as size, resonance, fixed compensation characteristic etc. To solve these problems, various static VAR compensator (SVC) configurations have been proposed. While some SVC's generate low order harmonics themselves, many lack the response time required for fast fluctuating loads. Further research has also led to the design of various active harmonic filters.

To reduce harmonics in a single phase system, Jou et al[10] proposed the active filter shown in Figure 31.

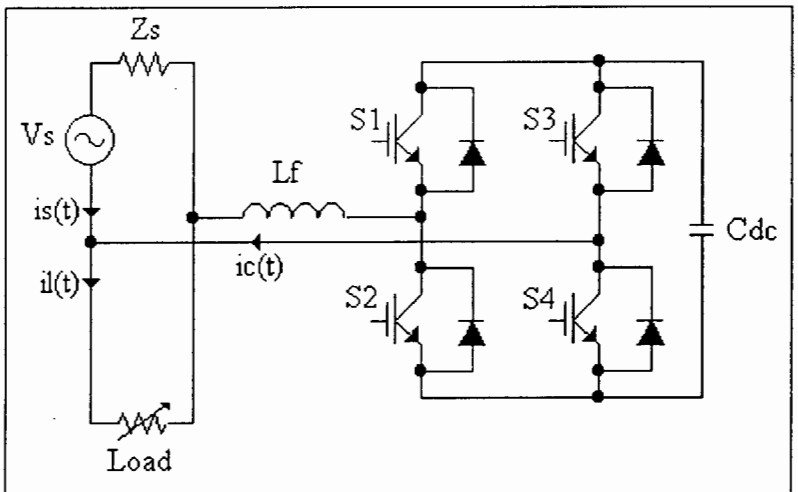

Figure 31: The Jou et al single phase active harmonic filter.

The filter consists of a full bridge inverter connected in parallel with the primary supply. An inductor L_f is used to ensure that the harmonic compensation current $i_c(t)$ injected back into the supply is *smooth*. Assuming the non-linear load current $i_L(t)$ is given as,

$$i_L(t) = \sum_{n=1}^{\infty} I_n \cdot \sin(n \cdot \omega \cdot t + \theta_n) \qquad \ldots(2)$$

Dividing the load current $i_L(t)$ into fundamental and harmonic components gives,

$$i_L(t) = I_n \cdot \sin(\omega \cdot t + \theta_1) + \sum_{n=2}^{\infty} I_n \cdot \sin(n \cdot \omega \cdot t + \theta_n) \qquad \ldots(3)$$

[9] Peng, FZ.; Akagi, H.; Nabae, A.; "A new Approach to Harmonic Compensation in Power Systems - A Combined System of Shunt Passive and Series Active Filters", IEEE TIA, Vol. 26, No. 6, Nov/Dec 1990

[10] Jou, HL; Wu, JC.; Chu, HY; "New single-phase active power filter", IEE Proc. Power Appl., Vol. 141, No. 3, May 1994

The compensation current $i_c(t)$ is then calculated by subtracting the real part of the load current at the fundamental frequency from the total load current $i_L(t)$.

$$i_c(t) = \sum_{n=1}^{\infty} I_n \cdot \sin(n \cdot \omega \cdot t + \theta_n) - I_1 \cdot \cos(\theta_1) \cdot \sin(\omega \cdot t) \qquad ...(4)$$

The voltage fluctuation ΔV_{DC} on the DC bus depends on the power rating of the filter and the load type. To ensure good harmonic compensation and high efficiency, the DC bus voltage is regulated. This is achieved by adjusting the amplitude of $i_S(t)$.

The Jou et al single phase active filter has two distinct advantages: it can force the current $i_S(t)$ to be a sine-wave even when the supply voltage V_S is distorted and; it can compensate for the harmonics of symmetrical and asymmetrical non-linear loads.

With this filter connected at the supply interface, the UPS could maintain a highly non-linear load and still ensure a THD of less than 5%.

4.3 Improving the transfer characteristic

A supply failure was reflected by the locally manufactured UPS, as a output voltage sag - sometimes accompanied by a glitch. Generally, sensitive loads cannot tolerate a voltage sag of 15% for more than 30 cycles[11]. Similarly, a total loss of supply can only be tolerated for at most a half cycle. Certain PC manufacturers quote hold-up times in the region of 50 milliseconds; third party reviewers of UPS's have shown this to be a very conservative estimate[12]. In either case, the locally manufactured UPS response is within the specifications for a sensitive load. However, the design objectives require tighter control of the output voltage.

The transfer characteristic can be improved by reducing the time taken to detect the supply failure[13]. The faster response by the detector could ensure that the output voltage is remains within the 1% regulation limit.

Another option is to use an online UPS configuration. In a true online UPS system, a supply failure will have little effect on the output waveform. This is because the output is powered from the battery via an inverter. The primary supply is used only to charge the battery pack.

4.4 Modifying the locally manufactured UPS

To modify the locally manufactured UPS to meet the design objectives would be a costly and complex procedure. It would require the addition of modules to shape the UPS input current, regulate and deglitch the output voltage, speed the transfer response etc. This would result in a larger, bulkier and inefficient system. The

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[11] The IEEE Orange Book, "Recommended Practice for Emergency and Standby Power Systems for Industrial and Commercial Applications", IEEE Std. 446, IEEE publication, 1987

[12] Bedford, M.; "Stormy weather - Lightning Protection", Computer Shopper, January 1995

[13] Shakarjian, DR.; Standler, RB.; "AC Power Disturbance Detector Circuit", IEEE Trans. Power Delivery, Vol. 6, No. 2, April 1991

alternative is a complete redesign around the objectives. The latter approach has been adopted and is now detailed further.

4.5 The proposed UPS topology

The block diagram of the proposed topology is given in Figure 32. The configuration is that of an online UPS. The method by which each UPS block satisfies the relevant design criteria is described in the following subsections.

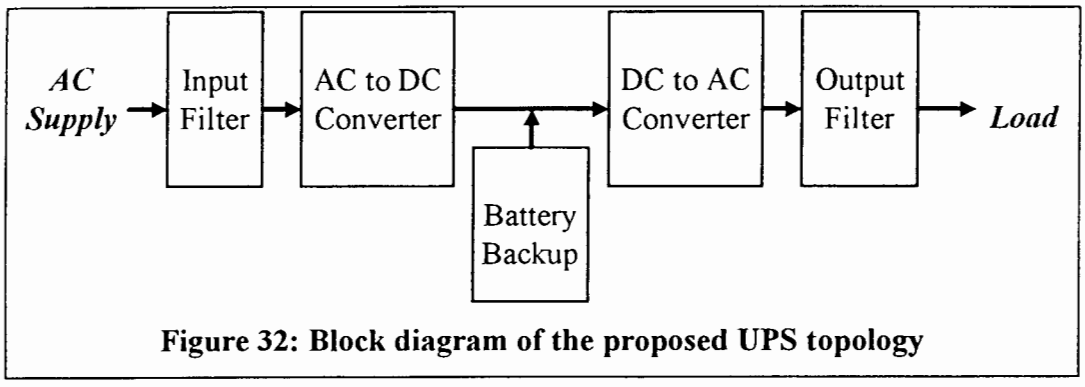

Figure 32: Block diagram of the proposed UPS topology

4.5.1 Input filter

The purpose of the input filter is to prevent the high frequency currents generated by the AC to DC converter from entering the AC power line. It is also attenuates spikes, surges, differential and common mode components which may be present on the input.

4.5.2 AC to DC converter

The output voltage of this converter must be larger than the incoming voltage to compensate for the voltage drops incurred by the DC to AC converter and output filter.

A basic AC to DC converter is the full bridge rectifier. The output voltage can be increased by powering the rectifier through a step-up transformer connected to the supply. The use of step-up transformer can avoided by replacing the lower bridge diodes *D2, D4* with capacitors. Unfortunately this method doubles the DC bus voltage, and increases device voltage ratings and bus ripple. In either case, the input power factor of the full bridge rectifier or voltage doubler is poor. An improved interface can be provided by increasing the AC side inductance[14]. The increased diode conduction interval reduces both the crest factor[15] and form factor[16]. A further improvement in the current waveform can be obtained using the arrangement shown in Figure 33.

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[14] Mohan, N.; Undeland, TM.; Robbins, WP.; "Power Electronics: Converters, Applications and Design", pp. 414-415, John Wiley & Sons Inc., 1989

[15] $CrestFactor = \frac{I_{s(peak)}}{I_s}$

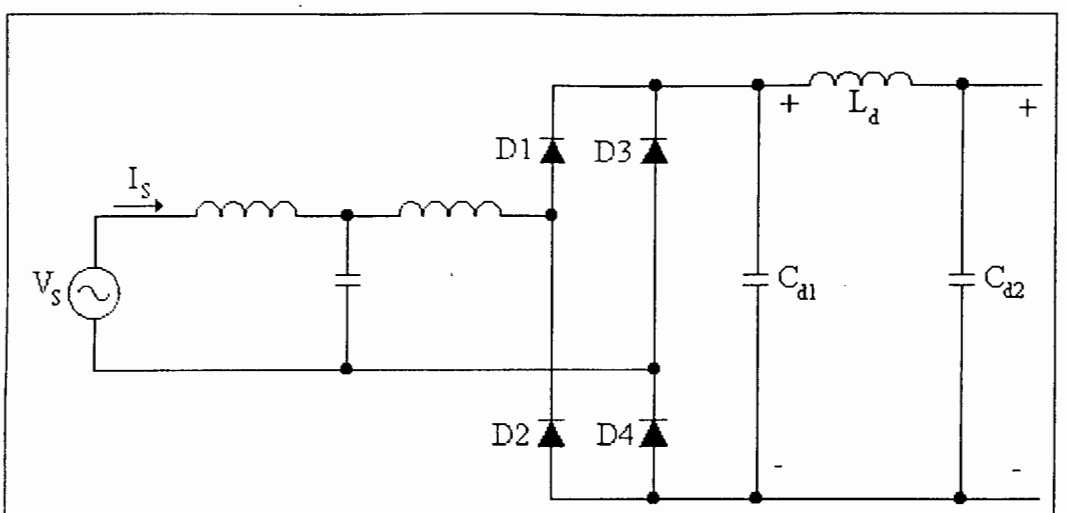

Figure 33: A passive filter to improve the line current I_s

By allowing a larger ripple V_{d1} on C_{d1} with $C_{d1} << C_{d2}$, the line current I_s is improved. The ripple V_{d1} is then filtered by the low pass filter L_d, C_{d2}. The disadvantages of this arrangement are cost, size, losses and the dependence of the average dc voltage of C_{d2} on the load current.

Even with the additional components, the full bridge rectifier cannot meet the 5% THD design objective. One option is to combine the rectifier and passive components with the active harmonic filter discussed previously[17]. The alternative is to combine the rectifier with a DC to DC step-up converter as illustrated in Figure 34[18]. Besides boosting and regulating V_d, the control circuitry can also ensure that the rectifier draws a sinusoidal current $i_s(t)$ at unity power factor from the primary supply $v_s(t)$.

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[16] $FormFactor = \dfrac{I_s}{I_{s(average)}}$

[17] Peng, FZ.; Akagi, H.; Nabae, A.; "A New Approach to Harmonic Compensation in Power Systems - A Combined System of Shunt Passive and Series Active Filters", IEEE TIA, Vol. 26, No. 6, Nov/Dec 1990

[18] A further rectifier-boost configuration for 3 phase systems is described by Zhao, Y.; Li, Y.; Lipo, TA.; "Force Commutated Three Level Boost Type Rectifier", IEEE TIA, Vol. 31, No. 1, Jan/Feb 1995

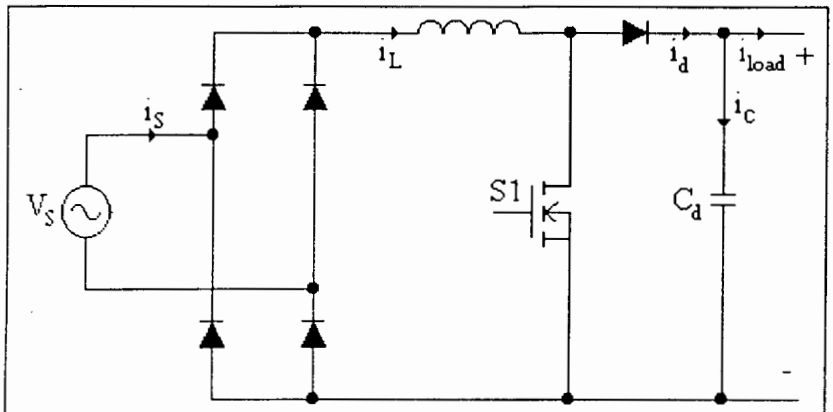

Figure 34: Active line current shaping using a DC to DC boost converter

The higher DC bus voltage improves efficiency by reducing the $i^2 \cdot R$ losses. An additional benefit of a higher voltage, is the increased energy storage of the DC bus capacitor ($E \propto V^2$) while still limiting the physical size of the capacitor[19].

Furthermore, if the DC bus voltage is higher than the output voltage, the energy stored in the DC bus capacitor can be used to maintain the load current during a supply failure. As the load current flows, the capacitor relinquishes its energy causing the bus voltage to drop. The amount of ride through time t_r provided by the bus capacitance C after a supply failure at time t_0 can be calculated as:

$$t_r = \frac{\pi - a\cos\left(\frac{\Delta V \cdot C \cdot \omega + \sqrt{2} \cdot I_{RMS} \cdot \cos(\omega \cdot t_o)}{\sqrt{2} \cdot I_{RMS}}\right) - \omega \cdot t_o}{\omega} \qquad \ldots(5)$$

where

$$\omega = 2 \cdot \pi \cdot f$$
$$i(t) = \sqrt{2} \cdot I_{RMS} \cdot \sin(\omega \cdot t)$$
$$\Delta V = Vdc_{t_o} - Vdc_{\min}$$

The ride through time t_r also relaxes the requirements of the supply failure detector. Computational complexity is reduced since a DC voltage level is measured instead of monitoring, point by point, the envelope of a sinusoidal waveform.

4.5.3 Battery Backup

If during a supply failure the DC bus is connected directly to the battery pack, it requires that the discharged battery pack voltage to be larger than the minimum peak

[19] Giles, W.; "Some solutions to PSU 'hold-up'", Product Focus, Electronic Eng., pg. 41, January 1994

load voltage - after the elapsed backup period. The number of series-connected batteries n required for a load voltage V_{Load} can be calculated from,

$$n = Round\left(\frac{V_{load} + V_{losses}}{V_{bat(discharged)}} + 0.5\right) \qquad ...(6)$$

Assuming a discharged battery voltage of 10V, a minimum peak load voltage of $\sqrt{2} \cdot 220V_{RMS} - 5\% \approx 296volts$ in a loss-less system, requires thirty batteries. Although basic in its implementation, the large battery backup pack has a number of significant disadvantages such as size, weight, extra capacity[20] and cost. The alternative is to use a lower battery pack voltage and boost it to the correct level through a DC to DC converter.

4.5.4 DC to AC Converter

The sinusoidal output voltage can be synthesised through either a half-bridge or full-bridge inverter (Figure 35).

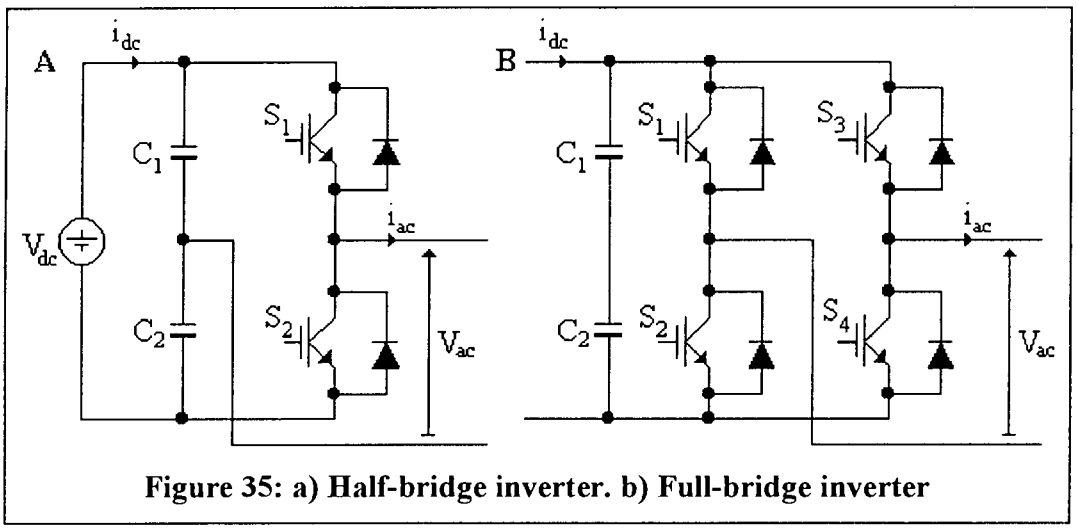

Figure 35: a) Half-bridge inverter. b) Full-bridge inverter

If in the steady state, $v_{ac}(t)$ from the half-bridge configuration is applied to an inductive load such as a transformer, capacitors C_1 and C_2 prevent saturation by blocking any DC current component. Unfortunately, the peak output is limited to $0.5 \cdot V_{dc}$. For the required output of $V_{ac} = 220V_{RMS}$, the half-bridge requires a DC bus voltage of at least 623V. Besides the increased cost associated with high voltage semiconductors, generating and maintaining such a high bus voltage would prove difficult for the AC to DC boost converter[21].

---

[20] Eg. Assuming a design objective requires 15 minutes of backup time. At 3kVA the DC bus current is 14 amps. Together, ignoring losses, this implies a battery pack amp hour (Ah) rating of 14*15/60=3.5Ah. The closest available battery is sized at 6.5Ah. The 3Ah extra capacity is an overdesign resulting in a cost increase.

[21] A higher bus voltage can be achieved using a *voltage boosted boost converter*. See AN19-14, Linear Technology's Linear Applications Handbook, Vol. 1, 1990

In the full bridge inverter, the DC bus voltage can be reduced to a minimum of 311V. This is at the expense of an extra two semiconductor switches S_3, S_4. At the same power level, the switch currents are halved. This is a distinct advantage at higher power levels as it requires less paralleling of devices.

In addition to determining the harmonic content of $v_{ac}(t)$, the PWM method used to control the switches S_1-S_4 will also influence the efficiency of DC to AC converter. These and other factors are discussed in the following section.

4.5.5 Output Filter

The purpose of the output filter is to ensure that the voltage supplied to the load is sinusoidal with less than 5% THD. The type of PWM switching strategy employed by the full bridge inverter defines the filter characteristic. Two switching strategies are considered namely: bipolar and unipolar PWM[22].

Refer to Figure 35. If bipolar PWM is used, the diagonally opposite switches (S_1,S_4) and (S_2,S_3) are driven together. As illustrated in Figure 36, the control signal for the first pair (S_1,S_4) is generated by comparing the modulation signal V_{mod} against the triangular waveform V_{switch}. The signal is then inverted and used to drive (S_2,S_3).

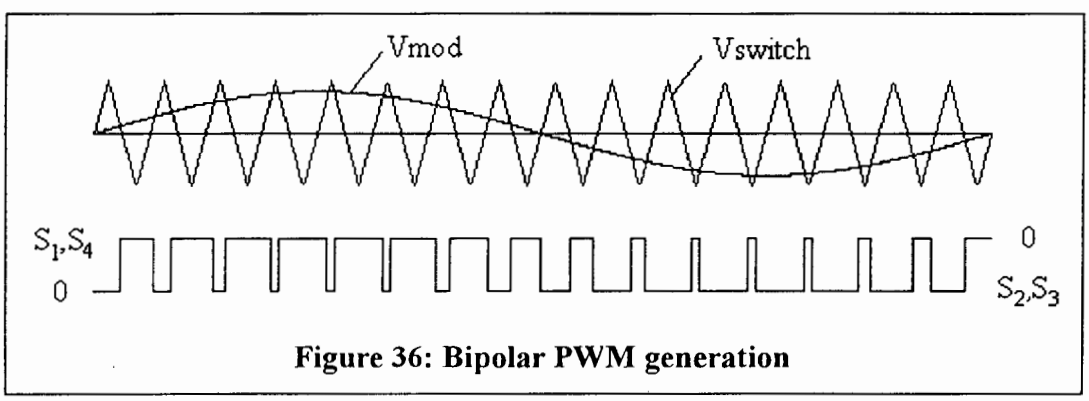

Figure 36: Bipolar PWM generation

From the harmonic spectrum given in Figure 37, the output filter is required to reduce the amplitude of the switching frequency harmonic $m_f = f_s / f_m$ by at least 26dB to achieve 5% harmonic distortion. The required attenuation increases further as components around $2m_f$, $3m_f$, $4m_f$.. are included.

[22] Other PWM methods are discussed in Prasad, N.; Ziogas, PD.; "Programmed PWM techniques to Eliminate Harmonics: A Critical Evaluation", IEEE TIA, Vol. 26, No. 2, March/April 1990

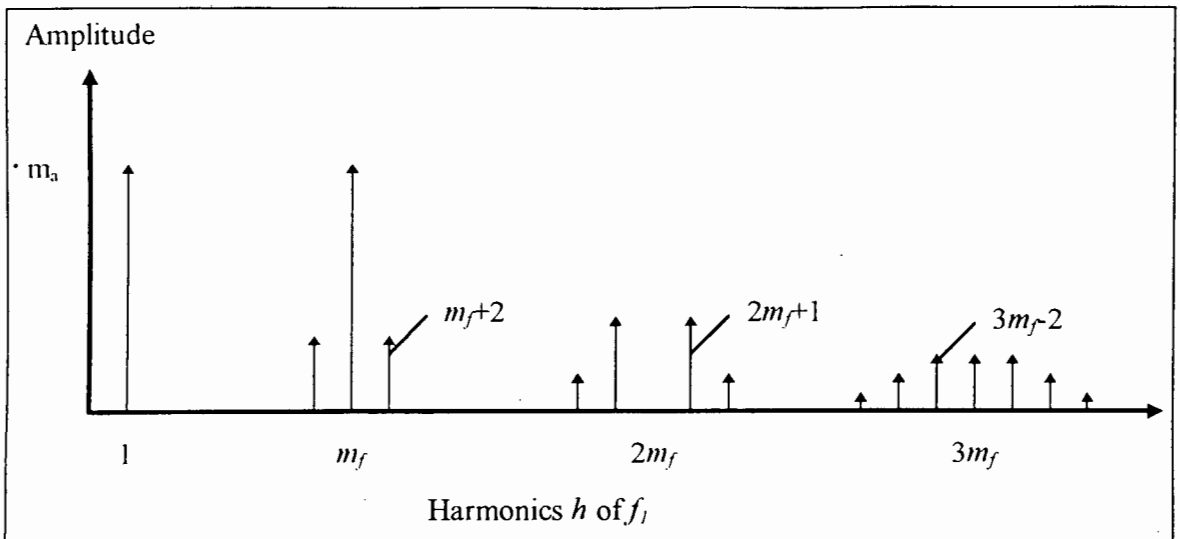

Figure 37: Normalised harmonic spectrum for bipolar PWM

Unipolar PWM is generated by comparing the triangular waveform V_{switch} against a positive V_{mod} to determine the (S_1,S_2) switching instants while a comparison against a $-V_{mod}$ controls (S_3,S_4).

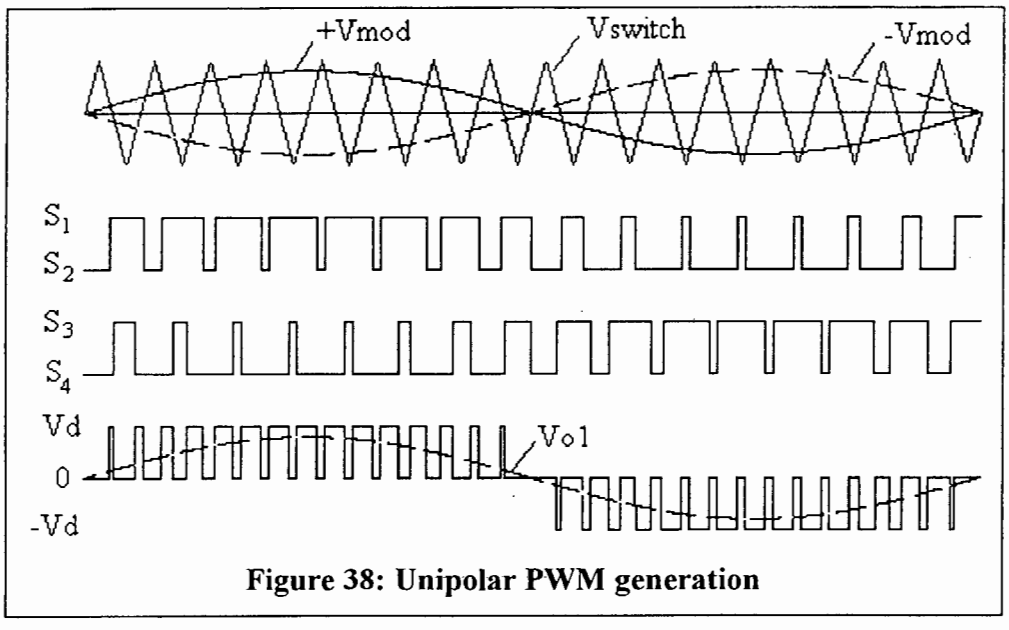

Figure 38: Unipolar PWM generation

As illustrated in Figure 38d, the output of the full bridge inverter is the summation of these switch control signals. Switching occurs between 0V and $+V_{dc}$ or between 0V and $-V_{dc}$ hence the term unipolar PWM as opposed to the $\pm V_{dc}$ switching of bipolar PWM. Therefore, the EMI generated by the unipolar driven bridge is less due to the reduced dv/dt at each switching instant.

Closer examination of Figure 38d reveals twice the number of discrete pulses per cycle as compared to bipolar PWM. The advantage of effectively doubling the switching frequency appears in the output harmonic spectrum (Figure 39) where the lowest harmonics appear as side-bands of twice the switching frequency.

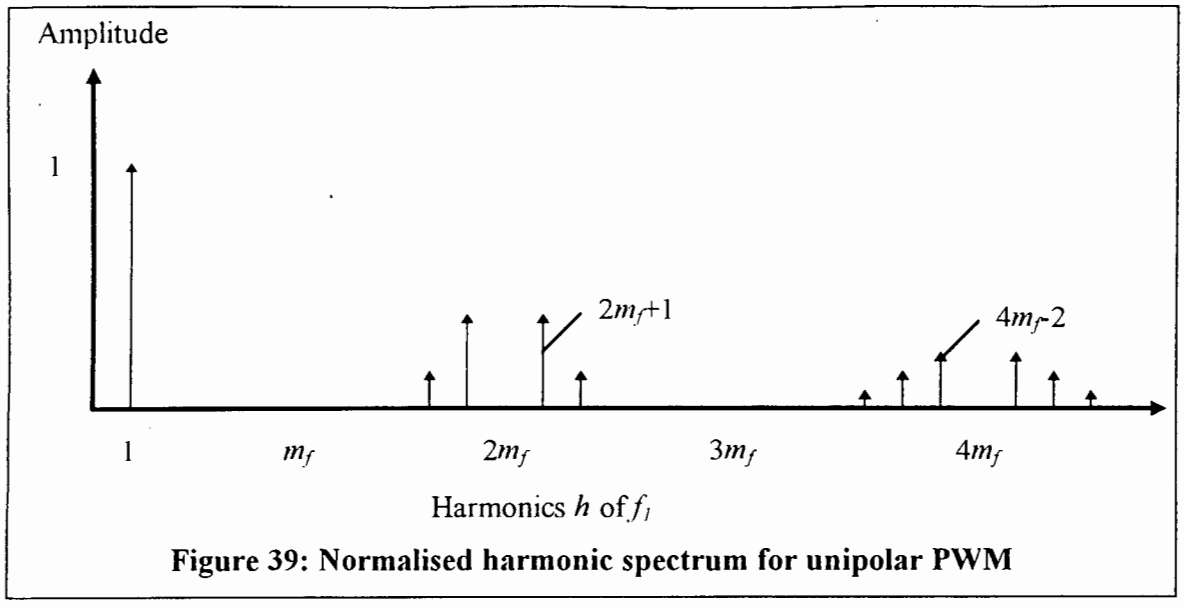

Figure 39: Normalised harmonic spectrum for unipolar PWM

The higher frequency components reduce the size and improve efficiency the output of the filter. With smaller filter components there is less energy storage. The lower energy storage limits output fault currents and the reduces filter input current. However, increasing the energy storage reduces the output impedance, assisting the output voltage under severe load changes. Either way, the design of the output filter is a compromise between harmonic and regulation requirements. The effects of the digital PWM implementation is covered in Appendix A while the filter design is continued in chapter 7.

To clarify, the complete power circuit of the proposed topology is shown in Figure 40.

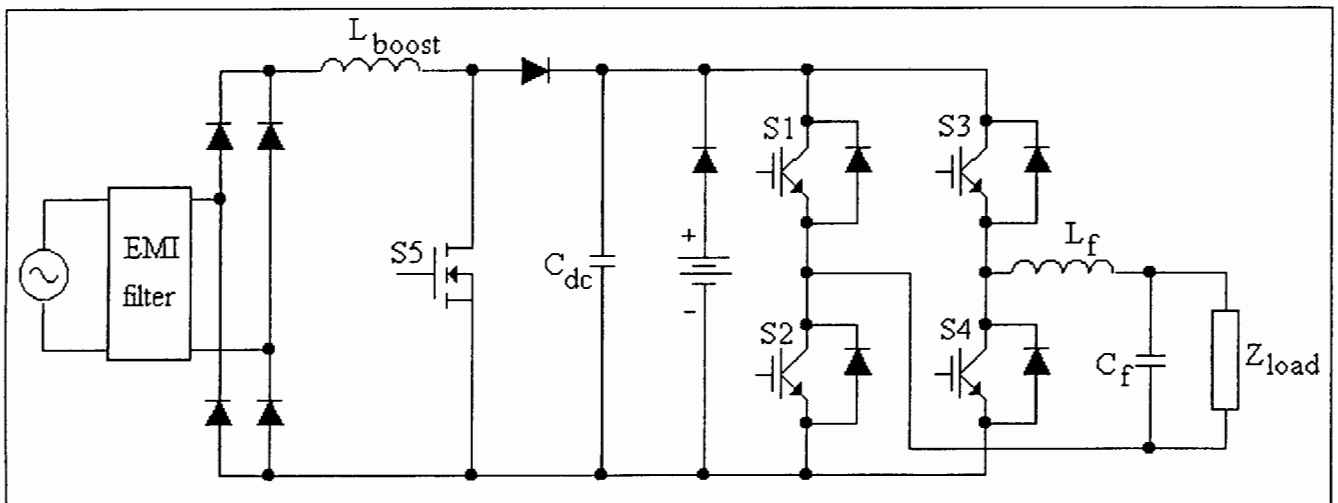

Figure 40: Power circuit of the proposed topology

The proposed topology is easily adapted to three-phase systems. Converting to three-phase requires an additional leg for both the rectifier and inverter. The UPS would then draw power from the supply at unity power factor whilst supplying the load at a

different power factor. Another application is as a single to three-phase converter. This is especially useful in rural areas where the provision of three-phase power is uneconomical[23]. Furthermore, the rate structure of a three-phase service is higher than that for a single-phase service. Therefore, single-phase to three-phase converters are excellent choices for situations where three-phase power is not available. With the additional inverter leg, the proposed system could supply several kilowatt. This is again the result of its unity power factor front-end extracting maximum power from the single-phase supply.

In the following chapters, the design of the various sub-sections are presented.

[23] Prasad NE.; Rahman, A.; Jakkli, R.; "Economic Single-Phase to Three-Phase Converter Topologies for Fixed and Variable Frequency Output", IEEE Trans. Power Elect., Vol. 8, No. 3, July 1993

5. Power Factor Corrector Design

5.1 Design specifications

The following specifications guided the design of the power factor corrector (PFC).

Table 1: AC to DC converter specifications

Parameter	Specification
Operating voltage	180..250V_{RMS}
Output power	> 3.5kW
Output voltage	380VDC (-5%, +0%)
Power factor	≈ 1
Total harmonic distortion	< 5%

5.2 Power factor correction techniques

Most PFC techniques using the boost topology are operated either in continuous or discontinuous inductor current modes with a constant or variable switching frequency.

5.2.1 Discontinuous-mode operation

The principle of a freely oscillating controller exploits the physical relationship between the voltage across and current through the boost inductor. It is only when the current in the boost inductor has gone to zero - hence the term "discontinuous mode" - that the semiconductor switch goes conductive.

The zero-current switching does away with the fast recovery diode's power-squandering reverse currents. If the triangular currents flow continuously through the inductor, the input current averaged over a high-frequency period is exactly half the peak high-frequency inductor current. If the peak currents are located along a low-frequency sinusoidal envelope, the input current available after filtering is also sinusoidal.

The process is illustrated by briefly analysing the inductor current waveform given in Figure 41.

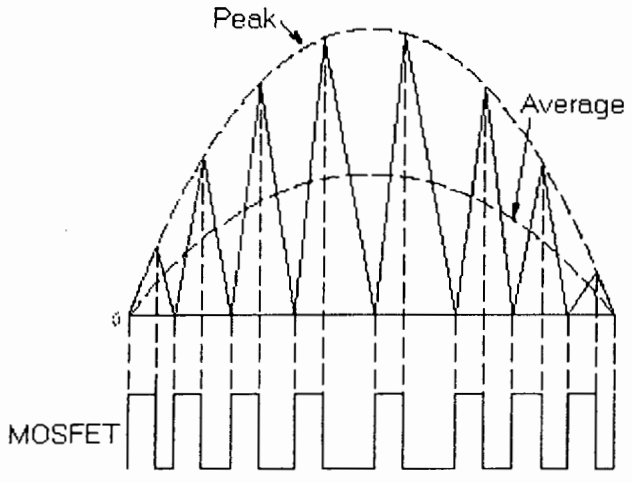

Figure 41: Discontinuous mode inductor current

With the boost switch enabled, the inductor current is given by

$$\frac{V_L}{L} = \frac{dI_L}{dt} \qquad ...(1)$$

The on-time of the semiconductor switch is controlled by the output voltage error amplifier. The on-time varies with line and load conditions but can be considered constant for a half-cycle because the voltage error amplifier bandwidth is rolled off to 0dB well below the line frequency. This prevents the voltage loop from attempting to correct for the DC bus ripple caused from the delivery of a sinusoidal current into the output capacitor[24].

Since...

$$V_L(t) = |V_{line}(t)| = \sqrt{2} \cdot V_{RMS} \cdot |\sin(\omega \cdot t)|$$

and...

$$dI_L = I_{peak}(t)$$

Therefore

$$I_{peak}(t) \propto V_L(t)$$

This relationship demonstrates that the instantaneous line current will track the instantaneous line voltage.

The required on-time $t_{ON}(t)$ is calculated as follows:

$$P_{in} = V_{RMS} \cdot I_{RMS} \qquad ...(2)$$

$$P_{out} = \eta \cdot P_{in} \qquad ...(3)$$

It has already been established that the peak inductor current is exactly twice the average current due to the zero-current switching. Therefore combining (2) and (3) yields,

$$I_{L(peak)} = 2 \cdot \frac{\sqrt{2} \cdot P_{out}}{\eta \cdot V_{RMS}} \qquad ...(4)$$

With the peak line voltage specified, the on-time is calculated from (1) as,

[24] Shimizu,T.; Fujita,T. et al; "A Unity Power Factor PWM Rectifier with DC Ripple Compensation", IEEE TIE, Vol. 44, No. 4, pp 447-455, August 1997

$$t_{ON(\max)} = \frac{L}{\sqrt{2} \cdot V_{RMS}} \cdot I_{L(peak)} \quad \ldots(5)$$

Combining (4) with (5),

$$t_{ON} = 2 \cdot \frac{L \cdot P_{out}}{\eta \cdot V_{RMS}^{\ 2}} \quad \ldots(6)$$

The on-time is adjusted slowly by the output voltage regulation loop. As already mentioned, the bandwidth of the voltage regulator is low so as to keep the on-time constant during the line cycle. The advantages of this approach are high noise immunity and simplicity since no squarer or sensitive multiplier circuitry is required.

The off-time $t_{OFF}(t)$ is a function of not only the input voltage but also the output voltage V_{out}. The time required for the inductor current to decrease from the peak value down to zero is expressed (assuming C is very large) as:

$$t_{OFF}(t) = \frac{L \cdot I_L(t)}{V_{out} - \sqrt{2} \cdot V_{RMS} \cdot \sin(\omega \cdot t)} \quad \ldots(7)$$

Substituting the time variant form of (4) into (7) yields,

$$t_{OFF}(t) = \frac{2 \cdot \sqrt{2} \cdot L \cdot P_{out} \cdot \sin(\omega \cdot t)}{\eta \cdot V_{RMS} \cdot (V_{out} - \sqrt{2} \cdot V_{RMS} \cdot \sin(\omega \cdot t))} \quad \ldots(8)$$

From (8), it is noted that the maximum load condition coincides with the lowest switching frequency while higher switching frequencies are associated with light loading and high line voltages.

The variable frequency operation (with the associated EMI / RFI problems) and troublesome peak current at increased power levels are avoided if the converter is operated in continuous mode.

5.2.2 Continuous-mode operation

A converter is operating in "continuous mode" if the inductor current remains above zero for the entire switching cycle. Constant frequency, average current mode control is now described.

Referring to Figure 42 (on page 36). The controller consists of an inner current control loop and external voltage regulation loop. The current loop minimises the error between a sinusoidal reference and the measured current. The need for a current measurement stems from the non-linear behaviour of the input current as a

consequence of the time dependent input voltage in continuous current mode (CCM)[25]. Hence only a continuous change of the duty ratio or operating frequency enables the boost converter in CCM to draw a sinusoidal line current. The current controller reference is formed by multiplying the rectified line voltage $V_{in}(t)$ with the voltage regulator output. Because $V_{in}(t)$ is included in the current loop reference signal, any distortion of this waveform is reflected as a corresponding distortion of the line current $I_{in}(t)$.

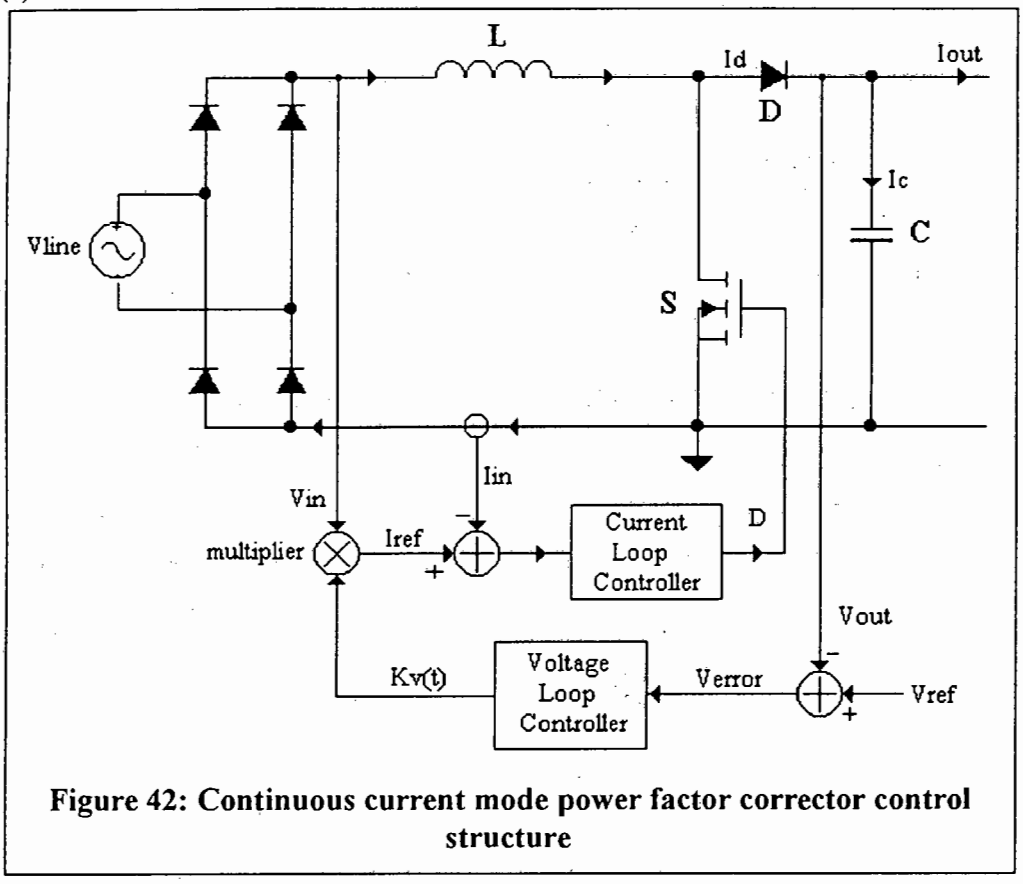

Figure 42: Continuous current mode power factor corrector control structure

The inductor current slope is usually small compared to the programmed level. Therefore peak current mode control is extremely susceptible to noise. Furthermore it is inherently unstable at duty ratios in excess of 50%. This instability results in a sub-harmonic oscillation[26] but is neutralised through the addition of "slope compensation" to the current reference. Ideally a compensating slope equal to half the inductor current down slope should be added to the reference[27]. This will ensure that all disturbances die out for any duty cycle up to 100%.

With a boost converter configuration, the inductor current down slope is given by $(V_{out} - V_{in})/L$ and thus varies as a function of the incoming line voltage. A fixed compensation slope will overcompensate much of the time, degrading performance and increasing the line current distortion.

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[25] For an approach using a pre-calculated sine-wave template rather than a current sensor, refer to: Sivakumar, S.; Natarajan, K.; Gudelewicz, R.; "Control of power factor correcting boost converter without instantaneous measurement of input current", IEEE TPE, Vol. 10, No. 4, July 1995

[26] Defined as a "deviation from the nominal operating point".

[27] Venable, HD.; "Current mode control", http://www.venableind.com/techpap/tpindex.html

The effect of (10) is to introduce a damping resistor in series with the inductor. Above f_c, the transconductance falls at 20dB/decade, increasing the control to output transfer function decline to 40dB/decade. The filtering on the current sense signal has a similar effect on the bandwidth of the transconductance.

The time-scale separation between the fast dynamics associated with $I_{in}(t)$ and the slow dynamics of $V_{out}(t)$ is readily exploited by the cascade control structure. This separation exists since $L << C$ and the requirement for a minimal phase displacement between $V_{in}(t)$ and $I_{in}(t)$. The current loop dynamics absorb the boost inductor. Consequently, the transfer function from the set-point to output voltage is reduced from a double to a single pole characteristic due to a current source driving the output capacitor. Thus the complexity of the voltage error amplifier and associated compensation network is reduced.

The voltage error amplifier compensation is driven by the need to keep the input current distortion to a minimum rather than by stability requirements. If input power is given by,

$$p_{in}(t) = \hat{V}_{in} \cdot \sin(\omega \cdot t) \cdot \hat{I}_{in} \cdot \sin(\omega \cdot t) = V_{in} \cdot I_{in} - V_{in} \cdot I_{in} \cdot \cos(2 \cdot \omega \cdot t) \quad ...(11)$$

Assuming the output capacitor C is large, the output power is,

$$p_{out}(t) = V_{load} \cdot i_d(t) \quad ...(12)$$

Equating (11) and (12) yields,

$$i_d(t) = I_{load} + i_c(t) = \frac{V_{in} \cdot I_{in}}{V_{load}} \cdot (1 - \cos(2 \cdot \omega \cdot t)) \quad ...(13)$$

Due to the low frequency power unbalance, the output capacitor always presents a voltage ripple at twice the line frequency. This cannot be compensated for by the voltage control loop without distorting the input current. Therefore the loop bandwidth must be low enough to attenuate the second line frequency harmonic. However the low-pass filter used in the feedback loop to remove the offending component results in the slow voltage-loop dynamics. During sudden load changes, the output voltage may overshoot or undershoot for several supply cycles. The poor voltage regulation can cause oscillations when a load with an under/over-voltage lockout is connected.

5.3 Controller selection

Ideally a single controller should be used for both the power factor converter front-end and the IGBT inverter back-end. The 80C552 microcontroller is able to calculate and generate both the boost switch and inverter PWM but only at a low switching frequency. At the maximum switching frequency of 4.5kHz (100% processor

utilisation), a boost inductor of 3mH capable of withstanding a peak current of 36 amps is required.

By increasing the operating frequency, the inductance is decreased (for same ripple current specification). This allows a powdered-iron, moly-permalloy powder (MPP) or ferrite core material to be used. These materials offer reasonably high saturation-flux density and low frequency-dependent losses. The increased operating frequency improves system dynamics, reduces the injected harmonic currents and simplifies filtering.

Although it is possible to simplify the control process[30] and thereby increase the operating frequency while still using the 80C552, an analog controller was selected as it offered greater flexibility in terms of the power component selection.

A number of manufacturers produce analog power factor controller ICs. Most are optimised for low power operation (<1kW) but can be utilised at higher power levels with some modification to the discrete components. They are listed in Table 2.

The devices listed, if correctly applied, also claim to satisfy the harmonic requirements as imposed by the International Electrotechnical Commission (IEC). See Appendix H.

Table 2: PFC manufacturers

Manufacturer	Device(s)
Linear Technology	LT1248*, LT1249
Micro-Linear	ML4812, ML4813, ML4819, ML4821, ML4824
Motorola	MC33368*, MC34261
Samsung	KA7514
SGS-Thomson	L4981
Siemens	TDA4814, TDA4817, TDA4862
Unitrode	UC3852, UC3853, UC3854*, UC3855

Devices marked with a "*" are/were available in sample quantities.

The MC33368 was rejected as it operates in discontinuous mode. Although the LT1248 uses average-current mode control, its switching frequency is tied to the maximum multiplier output current through R_{set}. The UC3854 was selected as it clamps this current at $2 \cdot I_{AC}$, thereby providing fold-back power limiting during brownouts and extreme low line conditions. It is also an industry standard device and supported by a number of second source suppliers (e.g. Toko TK3854).

The design of the discrete components around the UC3854 are detailed in Appendix B. While a complete device datasheet is given in Appendix D, product briefs for the LT1248 and MC33368D are also included.

[30] SGS-Thomson Microelectronics Application Note: Digital Power Factor Correction with Non-Sinewave Current

5.4 Power component selection

5.4.1 Full-bridge rectifier

At line low ($180V_{RMS}$) and assuming an overall system efficiency of 80%, the bridge rectifier must have a $I_{dAV} > (3500/0.8)/180 \cong 24.3A$. To withstand an over-voltage condition (+10%), $V_{RRM} > 1.1 \cdot 250 \cdot \sqrt{2} \approx 389V$. A Semikron SKB50/12 bridge was selected to satisfy the above requirements.

The SKB50/12 datasheet is included in Appendix D.

5.4.2 Boost inductor

A toroidal-shaped core was selected as it is the most efficient magnetically. The core specifications are given in Table 3.

Table 3: T520-28D core specifications

Iron-powder mix	28
Inductance (A_L)	$90nH/N^2$
Effective magnetic length (ℓ_m)	33.10cm
Effective magnetic area (A_e)	$10.5cm^2$
Effective magnetic volume (V_e)	$347.55cm^3$
Temperature range	-55°C to +125°C
Temperature coefficient	+415ppm/°C
Dimensions	OD=5.2", ID=3.08", Ht=1.6"

A distributed rather than a localised air-gap within the iron-powder eliminates the nuisance of a fringing field and its associated losses in nearby windings. It can also be used in place of ferrites[31] and iron-alloy laminations. The material is a cost-effective design alternative to moly-permalloy powder (MPP), high flux or sendust cores.

The -28 material mix was selected as it suitable for applications where the inductance must remain relatively constant over the entire load current range. The material is also able to store a large amount of energy with minimum saturation.

In Appendix B, the required inductance is calculated as 500uH at a ripple current of 1.8 amperes. The high peak current of 35 amperes and 100kHz operation of the converter necessitates the use of Litz-wire to combat the skin-effect[32]. A total of 800 metres of polyester ironide coated #17 wire was used to form a 40-stranded Litz-wire.

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[31] The term "ferrite" implies the material is iron-based, but that is not the case. Ferrite materials are actually grouped into nickel-zinc and manganese-zinc types.

[32] The skin effect is the phenomenon of increasing current-density concentration in the surface layers of the conductors as frequency increases; it arises because the reactance associated with the possible current paths is the smallest near the conductor surface. It is the depth at which the current density has decreased to 1/e (37%) of its value at the surface of the conductor.

Unfortunately a substantial winding area penalty must be paid to use Litz-wire. This is the result of its complex twisted structure and the presence of a large amount of internal insulation.

As the polyurethane core coating has a dielectric strength of at least 500 volts, the Litz-wire was wound directly onto the core. The second layer was however insulated from the first using glass-based Scotch 27 tape. This was done to prevent a voltage breakdown between the two winding layers.

The 500uH boost inductor design is covered in Appendix C.

The number of turns is calculated as $N = 93$. From $L = N^2 \cdot A_L$ and without a DC bias applied, an inductance of 778uH is calculated. Measurement using a HP4285A 75kHz-30MHz Precision LCR meter nonetheless revealed 853uH. The discrepancy between the calculated and measured value can be attributed to the winding construction.

Firstly A_L, with a tolerance of ±10%, is quoted for a single evenly distributed layer at 25°C. Assuming $A_L + 10\%$, an inductance of 856uH is attainable.

"*Secondly, an iron powder core with a number of turns which are not evenly distributed will produce a higher inductance reading than expected*"[33]. The apparent inductance is increased by both self-capacitance and leakage inductance.

5.4.3 Power switch

The voltage rating for a boost converter power switch must be greater than the output voltage. This is because any parasitic inductance between the switch, boost diode and DC capacitor will induce a voltage spike as the switch turns off. If the spike contains sufficient energy, the semiconductor will self-destruct due to avalanche breakdown. In addition, the sudden loss of a load will also increase the output voltage past its nominal value due to the slow voltage regulation loop response.

A 500V APT5012 was selected to satisfy the above requirement. The ISOTOP module encapsulates both the MOSFET switch and soft-recovery boost diode on a single aluminium nitride ceramic substrate.

The peak switch current is the sum of the maximum inductor current and diode reverse recovery current. In appendix B, the peak inductor current is calculated as $I_{peak} = 32A$. If a nominal di_F/dt=200A/us is assumed (≈150ns MOSFET turn-on), a reverse recovery current of 20 amperes is expected. Together, the 52 ampere peak pulse current is well within the APT5012 safe operating area.

The reverse recovery of the diode produces EMI that increases with di_F/dt. Elevated temperature also increases diode noise and thus EMI generation. The low lead

[33] "Iron-powder Core Selection Guide", Micrometals Inc., 1993

inductance and shielded construction of the APT5012 ISOTOP assists in the reduction and containment of this EMI.

The APT5012 datasheet is included in Appendix D.

5.4.4 Output capacitor

The selection of the output capacitor is determined by the peak-to-peak ripple voltage, RMS ripple current and the required lifetime of the capacitor.

In Appendix B, a minimum output capacitance $C_o = 3000uF$ was calculated based on a 20ms hold-up requirement. The peak-to-peak voltage ripple is calculated as:

$$V_{ripple(p-p)} = \frac{P_{nominal}}{V_{Bus}} \cdot \frac{1}{2 \cdot \pi \cdot f \cdot C_o} \cong 10V$$

The above calculation assumes the inverter load is resistive. As this assumption is incorrect and also to allow for capacitor tolerances and ageing effects, two 2000uF 450VDC electrolytic capacitors were selected. The additional 1000uF, together with the inverter DC bus monitor described later, should ensure that the voltage ripple remains within 10V. By minimising the voltage ripple, the harmonics injected into the line current through the PFC voltage regulation loop are reduced.

The life expectancy of a capacitor is a function of its temperature. The ripple current is responsible for the internal heating of the capacitor. For the boost PFC, it is approximated by[34]:

$$I_{RMS(f_s=100kHz)} = \frac{P_{nominal}}{\eta \cdot \sqrt{V_{bus} \cdot V_{RMS(\min)}}} \cong 14A \xrightarrow{100Hz} 11A$$

The calculated ripple current is within the specification of the selected capacitor. Assuming a worst-case ambient temperature of 50°C, the approximate life time is:

$$T_{int\_rise} = \left(\frac{I_{operating}}{I_{rated}}\right)^2 \cdot T_{ext\_rise} = \left(\frac{5.5}{8.4}\right)^2 \cdot 10 \cong 4.3°C$$

$$L = L_{rated} \cdot 2^{\frac{T_{rated} - T_{internal}}{10}} = 2000 \cdot 2^{\frac{(85+10)-(50+4.3)}{10}} \cong 33130hours$$

For a prototype system, the above life time figure is sufficient. In a military or space application, a life time exceeding 100,000 hours would be required.

[34] AMPSS® Reference Manual, Rev 2, January 1996

5.5 Estimating the efficiency of the power factor corrector

5.5.1 Calculation of the power loss in the bridge rectifier

Assuming the worst case operating conditions ($V_{LINE} = 180V_{RMS}$ and $P_{Load} = 3500W$), the losses are calculated as $P_{loss} = V_F \cdot I_{dAV(\max)} \cong 39W$. Mounted on the same 0.052°C/W PFC heatsink, the temperature is expected to rise by a further 2°C above ambient.

5.5.2 Calculation of the power loss in the boost inductor

The boost inductor power loss is the sum of the copper and hysteresis losses[35].

The total winding resistance is:

$$\Omega_{Total} = L_{(m)} \cdot \frac{R_{\#17AWG(\Omega/m)}}{N_{strands}} = 20 \cdot \frac{0.0166_{20°C}}{40} = 8.3m\Omega$$

Assuming 80% efficiency at a worst case line voltage of $180V_{RMS}$, the copper loss - ignoring the skin effect - is calculated as:

$$P_{copper} = I_{RMS}{}^2 \cdot \Omega_{Total} = 24.3^2 \cdot 0.0083 \cong 4.9W$$

The first step to determining the core loss finding the peak AC flux density.

$$B_{AC} = \frac{L \cdot I_{ripple}}{2 \cdot N \cdot A_e \cdot 10^{-8}} = \frac{500 \cdot 10^{-6} \cdot 1.75}{2 \cdot 93 \cdot 10.5 \cdot 10^{-8}} \cong 44.8gauss$$

The core loss for a type 28 material is approximated by ($f_s > 10kHz$):

$$P_{core} = 2.16 \cdot 10^{-9} \cdot f^{1.31} \cdot B_{AC}{}^{2.03} \cdot V_e = 2.16 \cdot 10^{-9} \cdot 100000^{1.31} \cdot 44.8^{2.03} \cdot 347.55 \cong 5.91W$$

The total inductor loss is therefore:

$$P_{Total} = P_{copper} + P_{core} = 4.9 + 5.91 = 10.81W$$

If a lower inductance is used e.g. 151uH, the core loss would be 28.75W due to the much higher ripple current (20%) and therefore AC flux swing.

The temperature rise that will result from a given core loss per unit volume is dependent on the core's effective surface area available to dissipate heat. Since volume is a cubed function and surface area is a squared function, a core's capacity to dissipate

[35] The inductor is the most efficient when the core and copper losses are equal. This also the point where the Q of the inductor is maximised.

heat per unit volume varies inversely with size i.e. large cores can dissipate less heat per unit volume than small cores for the same temperature rise.

The temperature rise for the T520-28D in free standing air can be estimated from the following (where S is the surface area of the toroid):

$$T_{Rise(°C)} = \left(\frac{P_{Total(mW)}}{S}\right)^{0.833} = \left(\frac{10806}{629}\right)^{0.833} \cong 10.7°C$$

The temperature increase above ambient is well below the recommended maximum of 125°C.

5.5.3 Calculation of the power loss in the diode and MOSFET

In circuits such as DC-to-DC converters, it is a simple matter to determine the semiconductor losses. However in a modulated converter, the calculation is more challenging since the waveforms vary continuously.

The power loss calculations for the APT5012JNU2 are adapted from the SGS-Thomson application note - AN603. The Mathcad document detailing these calculations is attached in Appendix J.

5.5.4 Calculation of the power loss in the DC bus capacitance and current sense shunt

The total power loss in the capacitors is calculated as:

$$P_{capacitor} = I^2 \cdot R_{esr} = 2 \cdot \left(\frac{11}{2}\right)^2 \cdot 0.070 \cong 4.2W$$

The power loss in the current sense at the minimum line voltage ($V_{LINE} = 180V_{RMS}$ and $P_{Load} = 3500W$) is:

$$P_{shunt} = I^2 \cdot R_{shunt} = 19.4^2 \cdot 0.02 \cong 7.6W$$

The inconvenience of such a small valued resistor and associated power loss can be reduced substantially through a current sense transformer (C.T.). A well designed C.T. has a wide bandwidth and low power loss. A C.T attached in-line with the PFC inductor will saturate since this current contains a significant DC component. The solution is two current sense transformers: the first is attached to the MOSFET drain while the second to the FRED anode. Their connection reconstitutes the true inductor current while simultaneously ensuring the cores reset after each pulse.

5.5.5 Analysis of the calculated PFC power loss

Table 4: PFC losses

Bridge rectifier	39W
Boost inductor	10.8W
Boost diode	137.4W
MOSFET	167.1W
Current sense shunt	7.6W
DC capacitors	4.2W
Total power loss	366.1W

The worst case efficiency for the PFC is around 90%. The MOSFET switching loss can be reduced by decreasing the gate resistance but at the expense of increased EMI generation due to the diode reverse recovery.

6. Inverter Design

The following factors are covered in the design of the full bridge DC to AC inverter: power switch specifications; gate drive considerations for IGBT modules; the calculation of the inverter losses and the physical layout of the power circuit.

6.1 Power switch specifications

Although the technology and control techniques exist to build a soft-switched full bridge DC to AC voltage source converter, the current efforts are aimed at the design of a hard switched system. It is hoped that a soft-switched system with lower device stresses and increased efficiency will be built in a follow-up project.

In a hard-switched converter, the power devices experience simultaneously high voltages and currents at both turn-on and turn-off leading to high switching stresses and losses. The power devices require a large (square) safe operating area (SOA) which compromises their speed and forward saturation voltage. The power devices and converter load must also withstand high $^{di}/_{dt}$ and $^{dv}/_{dt}$ - a characteristic of all hard-switching converters. Hence, to operate power devices under hard-switched conditions it is essential that the switching speed of the device can be controlled.

Currently the selection of switching device is a choice between either a bipolar junction transistor (BJT), insulated-gate bipolar transistor (IGBT), MOS-controlled thyristor (MCT) or a metal-oxide semiconductor field-effect transistor (MOSFET).

Since the BJT is a current controlled device, it requires a continuous base current to remain in the on-state. At high power levels, the low gain (β) of a power BJT results in a substantial base-drive current requirement (larger betas lead to a reduced breakdown voltage capability). Sometimes the devices are connected in a Darlington configuration to achieve a slightly higher current gain, but at the expense of a higher $V_{ce(sat)}$ and slower switching speed. Whether fabricated as a single unit or as a monolithic Darlington, a BJT has a significant storage time during the turn-off transition. Typical switching times are in the range of a few hundred nanoseconds to a couple microseconds.

The MOSFET is a voltage controlled device. No gate current flows expect during the transition from on to off or vice versa when the gate capacitance is being charged or discharged. This simplifies the design of the gate driver circuitry. Because the on-state resistance $r_{DS(on)}$ increases with the blocking voltage rating B_{VDSS}, the conduction losses increase. The MOSFET turns on and off very rapidly because it is a majority-carrier device - there is no stored charge that must be injected or removed as there is with a BJT. Together, the total losses (conduction + switching) can be less than an equivalent BJT only if the switching frequency is in excess of 30-100kHz.

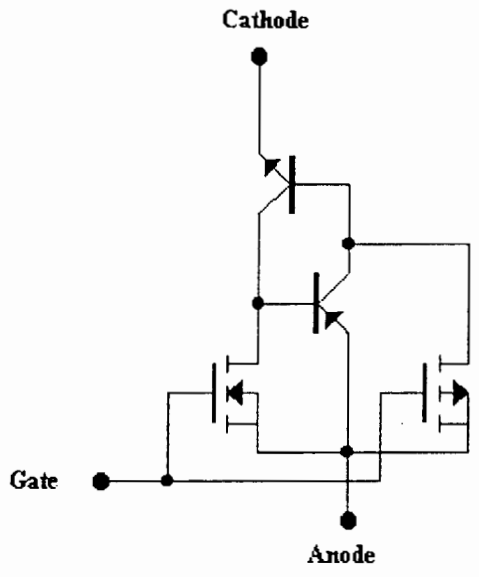

Figure 44: Equivalent circuit of the MCT

The MCT is a new device which combines the voltage and current capacity of a thyristor with a MOS-gated turn-on and turn-off (Figure 44). Turn-on is initiated by the gate signal but is completed regeneratively as in a thyristor. This results in a fast turn-on with a very good $^{di}/_{dt}$ capability but lacks the control required to limit the reverse recovery current in the free-wheeling diode. (A saturating inductor can be used to reduce the diode current.) Turn-off is achieved by shorting out a thyristor base-emitter junction. A successful turn-off requires all cells to turn-off at the same time to prevent current crowding. This imposes a gate rise time constraint. A clear advantage of a MCT is the lower conduction voltage - typically a third to one-half that of an equivalent IGBT.

The IGBT was developed specifically to meet the requirement for a robust, easy-to-use device, capable of switching high power at ultrasonic frequencies. It combines the speed, ease-of-drive and wide safe operating area of a MOSFET with the low saturation voltage of a bipolar device (Figure 45). This makes the IGBT the ideal semiconductor switch especially for motor drives, but also for welding applications and uninterruptible power supplies. Active inductive switching tends to favour the IGBT in medium to high frequency applications as its lower switching loss can out weigh the lower conduction loss of a MCT. An IGBT can also provide fault current limiting for a few microseconds allowing an orderly shutdown of the system. An MCT has no such mechanism - in a resonant circuit, shutdown would only be possible at the next zero-current or lower current interval.

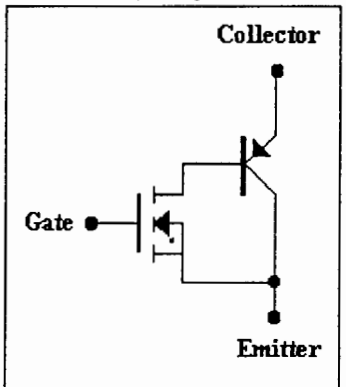

Figure 45: Equivalent circuit of an IGBT

From the above discussion, two half-bridge IGBT modules were selected for the DC to AC inverter. The required voltage and current ratings are now calculated.

When the switching frequency is well above the fundamental output frequency and the energy flow is bi-directional, the required collector current rating of each IGBT can be estimated from[36]:

$$I_C = \frac{2 \cdot P_{OUT}}{V_{DC(\min)}} \cdot \frac{K_L \cdot S_m \cdot U_w}{Ma \cdot \eta}$$

[36] Srajber, D.; "A short-cut to transistor current calculation in switch-mode power converters", SEMIKRON International Application News, 1994

where:

- P_{OUT} - Desired output power in watts.
- $V_{DC(min)}$ - Minimum expected DC bus voltage.
- K_L - Current ripple.
- S_m - Design safety margin.
- U_w - Overload factor.
- Ma - PWM modulation depth
- η - Inverter efficiency.

Assuming a worst case of P_{OUT} = 5000, $V_{DC(min)}$ = 330V , K_L = 10%, S_m = 20%, U_w = 1, Ma = 0.9, η = 85%, the peak IGBT collector current is calculated as ≈53 amps.

The DC bus is generated by rectifying the line voltage and then boosting it through a DC to DC converter. The configuration of the DC to DC converter is such that the output voltage will always be greater than or equal to the peak rectified line voltage. The DC bus voltage may also increase due to feedback from the load. A nominal ten percent increase is assumed in each case.

The maximum expected bus voltage (maximum line voltage=250Vrms) is calculated as:

$$V_{DC(\max)} = \sqrt{2} \cdot 250 \cdot \frac{110}{100} \cdot \frac{110}{100} \approx 424$$

Superimposed onto the bus are the voltage spikes generated at each switching instant due to the source impedance and stray circuit inductance ($L \cdot {}^{di}/_{dt}$). The stray inductance can be approximated through the following formula,

$$L_{stray} = 2 \cdot L_g \cdot \left(\log \frac{2 \cdot L_g}{r} - 0.75 \right) \cdot 10^{-7}$$

where L_g is the length of the conductor in metres and r is the conductor radius in metres.

A 100 amp conductor of length 10 centimetres between two 75 amp IGBT modules contributes 57nH to the total circuit inductance. If the load is short-circuited, the IGBT modules will limit the current to approximately 6 (homogeneous IGBT) to 10 (epitaxial IGBT) times the nominal current rating. During a short-circuit turn-off time of e.g. 500ns, the stray inductance will cause an over-voltage spike of $57 \cdot 10^{-9} \cdot 6 \cdot 75 / 500 \cdot 10^{-9} \approx 103V$. Adding this to the DC bus voltage of 424 volts results in a peak bus voltage of 527 volts.

To meet the above criteria (527V 53A), two half bridge Toshiba MG75J2YS40 (600V 75A) IGBT modules were selected.

6.2 Gate drive considerations for the IGBT modules

The correlation between the gate transfer characteristic and the switching performance of a MOSFET is well documented. A similar relationship exists for the turn-on of an IGBT, which is predominantly a majority carrier phenomenon. The MOSFET input stage of the IGBT drives the P-N-P transistor output stage and is therefore greatly affected by the gate drive signal. Increasing the gate drive voltage or decreasing the series resistance increases the rate at which the MOSFET input capacitance is charged. This results in a faster turn-on of the IGBT and a dramatic decrease in the turn-on switching loss.

Turn-off of an IGBT is determined by its bipolar characteristics. The removal of the gate charge exerts little influence on the minority carriers stored in the *n*-epi region because they recombine at a rate determined by the carrier lifetime. The gate drive thus has only a minor influence on the turn-off losses of the IGBT, while playing a major role in determining the switching losses at turn-on.

The switching losses is only one parameter that must be considered when designing the gate drive for a hard switch inverter circuit. The other parameters are:

- The effect of the inverse diode recovery time on switching loss and voltage transients.

  During turn-on, the diode recovery $^{di}/_{dt}$ combined with the DC loop inductance produces a recovery voltage transient. This recovery voltage transient can be limited to the rated breakdown voltage of the diode and IGBT in parallel with it, by increasing the gate resistance. A trade-off between this voltage overshoot and the turn-on losses is therefore necessary.

- The effect of noise generated by the inverse diode on control and protection circuits.

  A very low series gate resistor can cause unacceptable ringing during the diode recovery. The stray inductance and parasitic capacitance can combine to form a resonant circuit which will then oscillate. The electrical noise (EMI) thus produced can then interfere with the control and protection circuits. This can be solved by increasing the gate resistance, but the solution is in direct conflict with the reduction of the switching losses.

- DC loop inductance and voltage.

  The turn-off transient voltage is also caused by $^{di}/_{dt}$ induced voltage across the stray circuit inductance as the current changes its path from the conducting IGBT to the free-wheel diode. As noted previously, the gate drive has only a minor influence over the current fall, while the minority carrier lifetime has a significant impact on the turn-off losses and current $^{di}/_{dt}$. The turn-off switching time and energy are much lower in a high speed IGBT device than in a low saturation device . This

causes a higher voltage to be induced across the device by the loop inductance. A snubber circuit may be required contain this turn-off voltage transient.

- Short circuit protection.

  It has been shown that the ability of an IGBT to withstand a fault current can be improved by reducing the gate voltage applied to the device[37]. However, a reduction in the gate drive voltage should be accompanied by a reduction in the series gate resistor to avoid increasing the turn-on losses. Assuming a fault occurs, the rapid rise of current will pull the IGBT out of its full conduction state. The rise in the collector-emitter voltage V_{ce} will cause a current to flow through the Miller capacitance C_{cg}. If the gate resistance is high, the gate-emitter voltage V_{ge} will increase resulting in a much higher current. By lowering the gate resistance, V_{ge} can be clamped thereby reducing the fault current magnitude significantly. The lower fault current levels and therefore losses enable the device to better negotiate through the fault condition. This increases the device short-circuit endurance time, allowing the protection circuits more time to react.

- Off-state $^{dv}/_{dt}$ protection.

  It is quite common practise to apply a negative voltage to the gate of the IGBT when it is required to be off, to ensure that the gate voltage cannot rise above the threshold level. Whether this is necessary will depend on the level of the gate threshold voltage, the ratio of the Miller capacitance C_{cg} to C_{ge} and the maximum $^{dv}/_{dt}$ across V_{ce} that the IGBT is expected to withstand.

To simplify the inverter system and increase UPS reliability, two Semikron SKHI-21 IGBT/MOS drivers were selected to drive the IGBT modules.

To optimise switching performance, each driver includes a dual low impedance, high current, fully isolated, gate driver with separate turn-on and turn-off resistor values. The dead-time and over-current monitoring (through V_{CE}) is adjusted through a number of external components. Also included is a fault memory which can be used to inform the control system through the error signal. Each driver also only requires a single +15 volt power supply - this removes the need for a separate isolated supply for the upper IGBT.

[37] Castino, G.; Dubhashi, A.; Clemente, S.; Pelly, B.; "Protecting IGBT's against a short circuit", First Annual Motion Contr. Tech. Conf., October 1990

6.2.1 The calculation of the external gate driver components

The connection of the various external components for one half of the SKHI-21 driver is given in Figure 46. The component values are duplicated in the second driver half.

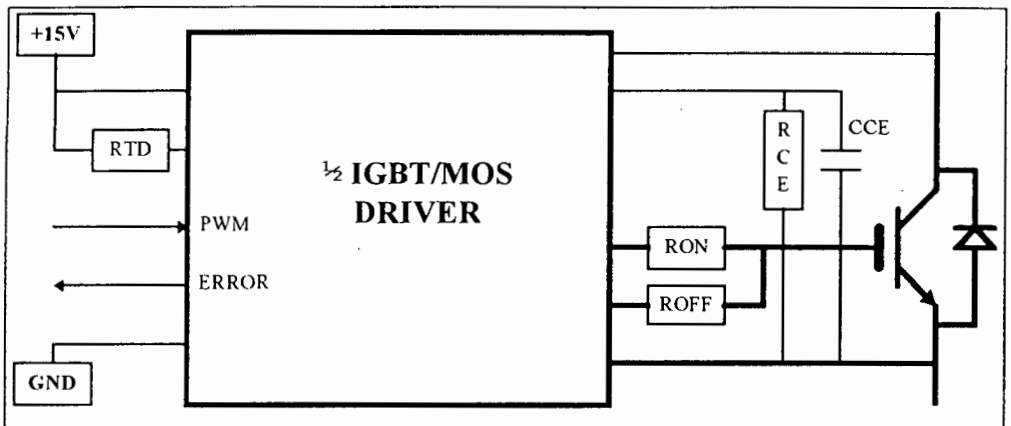

Figure 46: The connection of the external IGBT/MOS driver components

Using the graph of switching time versus gate resistance, the following initial values are selected for a turn-on of 350ns and turn-off of 470ns. Later, based on experimental data, the values may be increased to reduce the diode recovery current and the turn-off voltage spikes.

$$R_{ON} = 33\Omega \qquad R_{OFF} = 33\Omega$$

After establishing the turn-off time, the dead-time (µs) is calculated as follows:

$$\lambda_{TD} = 2.7 + 0.13 \cdot R_{TD}(k\Omega)$$

The recommended value of $R_{TD}=0\Omega$ is selected - the dead-time is therefore 2.7µs. The over-current / short-circuit monitoring is controlled through R_{CE} and C_{CE}. If the reference $V_{CE(ref)}$ is exceeded while the IGBT is in the on-state, the IGBT is turned off and the error signal activated. The reference $V_{CE(ref)}$ is calculated as follows:

$$V_{CE(ref)} = \frac{9 \cdot R_{CE}(k\Omega) - 25}{10 + R_{CE}(k\Omega)}$$

The saturation voltage $V_{CE(sat)}$ for the MG75J2YS40 at $I_C=75A$ and $V_{GE}=15V$ is given as 3.5 volts. To prevent false triggering, the reference level was placed slightly higher at 4.5V ($R_{CE}=15k\Omega$).

The inhibit time for V_{CE} monitoring is a function of C_{CE}.

$$\lambda_{CE}(\mu s) = C_{CE}(nF) \cdot \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)}$$

To ensure that the IGBT is turned on completely, the inhibit time is placed at 2.3μs (C_{CE}=*390pF*). The complete datasheet for the SKHI-21 driver and schematic is included in the appendix.

6.3 DC bus capacitor specifications

Directly or indirectly, over-stressed capacitors are involved in most circuit failures. Before the capacitor ultimately fails, it can directly contribute to the destruction of the switching devices and so mask the prime failure mechanism. It is therefore necessary to define the capacitor specifications to prevent such failure.

The inverter ripple current ΔI_C consists of a DC component - which is responsible for the real power transfer from the DC bus to the AC load - a large sinusoidal component at twice the fundamental and further components at multiples of the fundamental and switching frequency. The root mean square value is given by,

$$I_{C(RMS)} = \sqrt{I_{1(RMS)}{}^2 + I_{2(RMS)}{}^2 + .. + I_{h(RMS)}{}^2}$$

It can be shown that $I_{C(RMS)}$ = 26.46 amps. To meet the expected ripple current, four capacitors with the following specifications are connected in parallel (Table 5).

Value		*1000uF*
Capacitance tolerance		*-10%, +50%*
Voltage		*450V maximum*
Temperature range		*-55℃ to 85℃*
Life expectancy (rated voltage at 40°C)		*>200 000 hours*
Ripple current	@ 30°C	*13.42A*
	@ 50°C	*12.2A*
	@ 70°C	*9.15A*
	@ 85°C	*6.1A*
ESR (at 100Hz and 20°C)		*130mΩ*

Table 5: DC bus capacitor specifications

6.4 Estimating the efficiency of the inverter

The overall efficiency of the inverter system is determined from the sum of the semiconductor and DC bus capacitor power losses. The power losses in the IGBT switch and inverse diode are used to determine the required thermal resistance of the heat sink. This will ensure that the maximum junction temperature is not exceeded. Later the accuracy of the theoretical calculations are verified experimentally.

6.4.1 The calculation of the power dissipation in the IGBT switch and diode

The total energy dissipation may be subdivided into the turn-on energy W_{ON}, conduction energy W_{COND} and turn-off energy W_{OFF}. The total power dissipation P_{LOSS} for the IGBT and inverse diode is the energy dissipation of each pulse summed over a complete output period.

$$P_{LOSS} = \frac{1}{T} \cdot \sum_{t=0}^{T} \left(W_{ON} + W_{CON} + W_{OFF} \right)$$

P_{LOSS} is also dependent on the load power factor. Conduction losses occur due to the voltage drop across the IGBT switch and diode. The conduction loss in the IGBT increases while the conduction loss in the inverse diode decreases as the load power factor approaches unity. This results in a greater P_{LOSS} since the voltage drop across the IGBT is higher than that of the inverse diode. This is illustrated in the following section.

6.4.1.1 The calculation of the total conduction losses

The IGBT on-state voltage changes little between room temperature and the maximum junction temperature. This is due to the combination of the positive temperature coefficient of the MOSFET section and the negative temperature coefficient of the voltage drop across the BJT drift region. These voltages are however functions of the current flow through the devices and can be approximated by the following linear relationships.

For the IGBT switch:

$$v_{CE}(i_c) = V_T + i_c \cdot R_T = 1.7 + i_c \cdot \frac{1}{75}$$

Similarly, the voltage drop across the inverse diode is given by:

$$v_D(i_d) = V_D + i_d \cdot R_D = 1.28 + i_d \cdot \frac{1}{180}$$

The inverter conduction losses are calculated using the method presented in the Semikron handbook. The method is based on the probability of the an inverter switch receiving an ON signal. It therefore does not require exact knowledge of the PWM

switching patterns. The resultant expressions are easy to calculate and compare favourably with the measured losses.

The conduction loss for the IGBT switch is given by:

$$P_{IGBT} = \frac{V_T \cdot I_r}{\pi \cdot \sqrt{2}} \cdot \left(1 + \frac{\pi}{4} \cdot M_a \cdot \cos(\phi)\right) + \frac{R_T \cdot I_r^2}{2 \cdot \pi} \cdot \left(\frac{\pi}{2} + \frac{4}{3} \cdot M_a \cdot \cos(\phi)\right)$$

Similarly, the inverse diode conduction loss is given by:

$$P_{DIODE} = \frac{V_D \cdot I_r}{\pi \cdot \sqrt{2}} \cdot \left(1 - \frac{\pi}{4} \cdot M_a \cdot \cos(\phi)\right) + \frac{R_D \cdot I_r^2}{2 \cdot \pi} \cdot \left(\frac{\pi}{2} - \frac{4}{3} \cdot M_a \cdot \cos(\phi)\right)$$

M_a is the PWM modulation amplitude, $I_r = 2 \cdot I_{peak}$ and $\phi = a\cos(pf)$. The total inverter conduction losses are calculated by summing the losses across all devices ($M_a=1$, $pf=1$, $I_{peak}=15.4A$).

$$P_{LOSS} = 4 \cdot (P_{IGBT} + P_{DIODE}) \approx 279.6W$$

The effect of the load power factor on the above conduction loss at various values of M_a is illustrated in Figure 47.

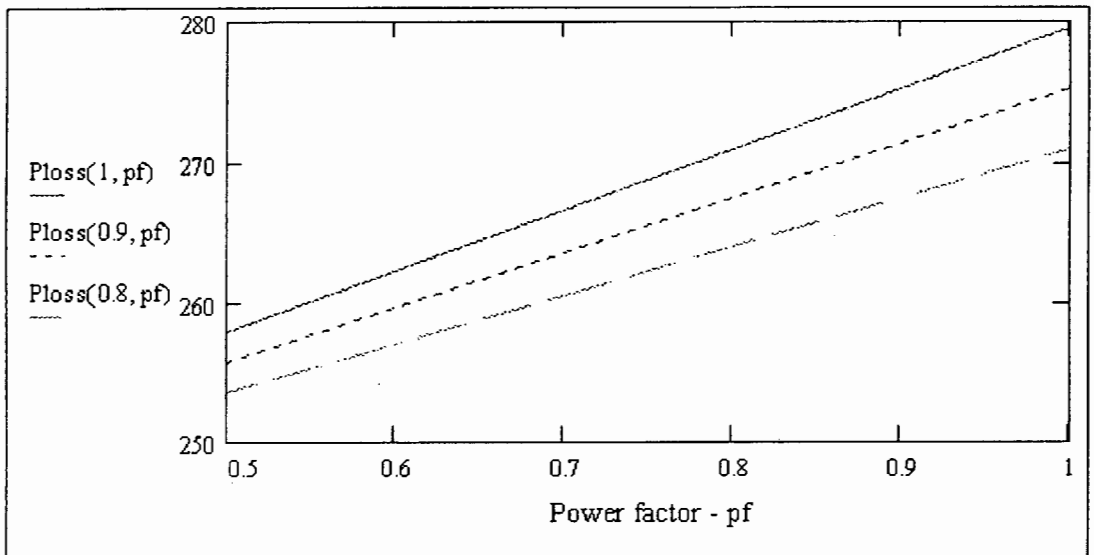

Figure 47: The inverter conduction loss versus load power factor

From the above graphic, it can be seen that a poor load power factor will benefit the UPS by reducing the inverter conduction loss and increasing system efficiency.

6.4.1.2 The calculation of the total switching losses

The IGBT turn-on W_{ON} and turn-off W_{OFF} dissipation is different for each current pulse. They are a function of the collector current, gate resistance, supply voltage, junction temperature and circuit layout. The exact values can only be measured in a

particular circuit configuration. Usually the manufacturer includes graphs of W_{ON} and W_{OFF} as a function of collector current and gate resistance but unfortunately these have been omitted from the Toshiba MG75J2YS40 datasheet. Therefore the switching loss in the IGBT can be approximated by the following expression:

$$P_{sw(IGBT)} = 2 \cdot V_{DC} \cdot I_{\max} \cdot f_s \cdot \left(t_{on} + t_{off}\right)$$

With a switching frequency of 6.2kHz and nominal bus voltage of $V_{DC} = 380$, the total IGBT switching losses is $P_{sw(IGBT)} \approx 202.17$ watts. Since it is assumed that the maximum current is occurs at each switching transition, the predicted switching loss will be higher than the measured loss.

The turn-on energy dissipation W_{ON} in the inverse diode is small compared to the turn-off energy dissipation W_{OFF} and is therefore neglected in the following analysis. From the MG75J2YS40 datasheet, I_{rr} and t_{rr} are determined as 3.9A and 71ns respectively at maximum current. The total inverse diode switching loss is $P_{sw(DIODE)} \approx 1.32$ watts.

6.4.2 The calculation of the power loss in the DC bus capacitor

The equivalent series resistance (ESR) is a lumped value representing all real power losses including dielectric and leakage losses within the capacitor[38]. In high frequency power supplies, the rapidly changing currents combined with the capacitor ESR contribute significantly to the DC bus voltage ripple $\Delta V_{DC} = \Delta I_C \cdot R_{ESR}$. The power loss in the DC bus capacitor is calculated from,

$$P_{loss(CAP)} = \Delta I_C{}^2 \cdot R_{esr}$$

Using $\Delta I_C = 26.46$ amps and $R_{esr} = 130m\Omega / 4$, the power dissipation distributed across all four capacitors at maximum load is $P_{loss(CAP)} = 22.75$ watts. This power loss increases the internal temperature of the bus capacitors, thereby decreasing their life expectancy and reducing the UPS reliability. For a longer life, capacitors with a higher ripple current rating or more paralleled capacitors should be used.

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[38] $ESR = tsr + \dfrac{R_p}{1 + \omega^2 \cdot R_p{}^2 \cdot C^2}$ where tsr is the true series resistance and R_p comprises the leakage resistance and dielectric loss due to molecular and interfacial polarisation.

6.4.3 Analysis of the total calculated power dissipation in the full bridge inverter

Total conduction loss	279.6W
Total switching loss	203.49W
DC bus loss	22.75W
Total dissipation	505.84W

Table 6: Analysis of the inverter power dissipation

The expected efficiency of the full bridge inverter is ≈90%. As revealed by Table 6, the switching loss contributes ≈40% to the total inverter power dissipation. The switching loss may be reduced by decreasing the switching frequency but at the expense of a lower output waveform resolution. This will also place the harmonic components closer to the fundamental, thus increasing the size (and possibly order) of the output filter. An alternative is to reduce the IGBT turn-on and turn-off times.

6.5 Thermal design of the inverter heatsink

IGBTs are thermally limited. They must be mounted on a heatsink that ensures the junction temperature is below the rated maximum under the worst case condition of maximum power dissipation and maximum ambient temperature. The task of selecting the device-heatsink combination which results in optimum utilisation is referred to as "*thermal design*".

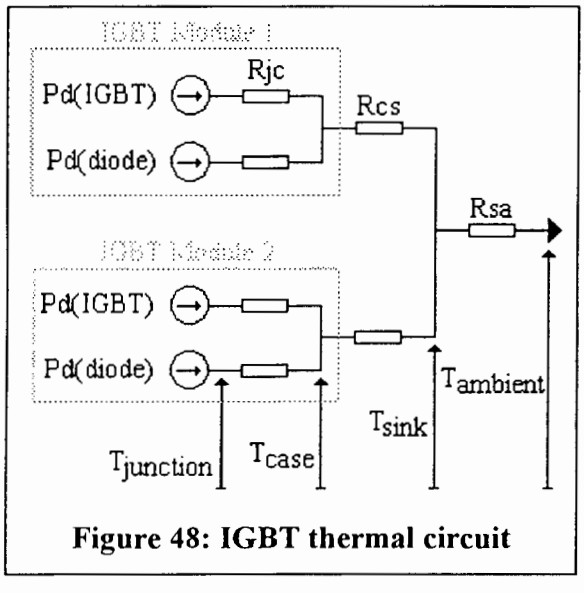

Figure 48: IGBT thermal circuit

In Figure 48, the total thermal resistance, $R_{\theta ja}$ is the sum of the internal junction-to-case thermal resistance $R_{\theta jc}$, plus the case-to-heatsink thermal resistance $R_{\theta cs}$, plus the sink-to-ambient thermal resistance $R_{\theta sa}$.

$$R_{\theta ja} = R_{\theta jc} + R_{\theta cs} + R_{\theta sa}$$

From the MG75J2YS40 datasheet:

$R_{\theta jc}$(IGBT) = 0.35°C/W
$R_{\theta jc}$(diode) = 0.83°C/W

A thin layer of thermal grease, correctly applied to the mating surface between the IGBT module and heatsink, should result in a $R_{\theta cs}$ of 0.005°C/W.

From the previous section, the theoretical power losses in the IGBT and diode are (per module):

$$P_{d(IGBT)} = 115.8475W$$
$$P_{d(diode)} = 4.925W$$

The temperature increase across the thermal resistances due to device dissipation is therefore:

$$\Delta T_{jc(IGBT)} = 115.8475 \cdot 0.35 = 40.55^{\circ}C$$
$$\Delta T_{jc(diode)} = 4.925 \cdot 0.83 = 4.09^{\circ}C$$
$$\Delta T_{cs} = (2 \cdot 115.8475 + 2 \cdot 4.925) \cdot 0.005 = 1.21^{\circ}C$$

The total semiconductor power dissipation for the inverter bridge is $P_{d(total)} = 483.1W$. The worst-case ambient temperature within the UPS cabinet is assumed to be $T_{a(max)} = 45°C$. The maximum junction temperature is placed at $T_{j(max)} = 125°C$, below the manufacturer's maximum of 150°C. The required thermal resistance of the heatsink $R_{\theta sa}$ is now calculated as:

$$R_{\theta sa} = \frac{T_{j(\max)} - (\Delta T_{jc(IGBT)} + \Delta T_{cs} + T_{a(\max)})}{P_{d(total)}} = \frac{125 - (40.55 + 1.21 + 45)}{483.1} = 0.079^{\circ}C/W$$

In the laboratory, only cut lengths of heatsink were available. The closest match to the required thermal resistance was $R_{\theta sa} = 0.27°C/W$. To meet the required $R_{\theta sa} = 0.079°C/W$, an air duct was constructed around the heatsink. An AC motor fan (more reliable than the DC equivalent) was then attached to the duct. To maximise the effect of forced cooling, the duct design aimed at minimising air turbulence while increasing the velocity of air over the cooling fins. As the manufacturer's specification did not include forced-cooling data for the particular heatsink the following experimental set-up was used to determine the thermal resistance.

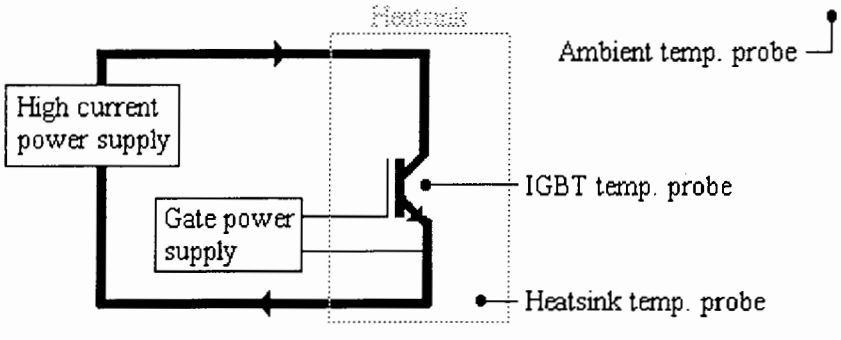

Figure 49: Calculation of the heatsink thermal resistance

In Figure 49, a high current power supply is connected across the IGBT collector - emitter terminals. A separate 15 volt supply is used to maintain the gate voltage. The heatsink was measured at its hottest point (under the IGBT) by a LM35D temperature probe inserted from beneath. The voltage across and current through the IGBT were recorded by an average responding voltmeter and LEM module respectively. To ensure accurate calibration results, the mounting and position of the heatsink during the experiment was chosen so as to mimic the actual installation within the UPS cabinet. The experimental results for a 100W dissipation are illustrated in Figure 50 and Figure 51 for natural and forced cooling respectively.

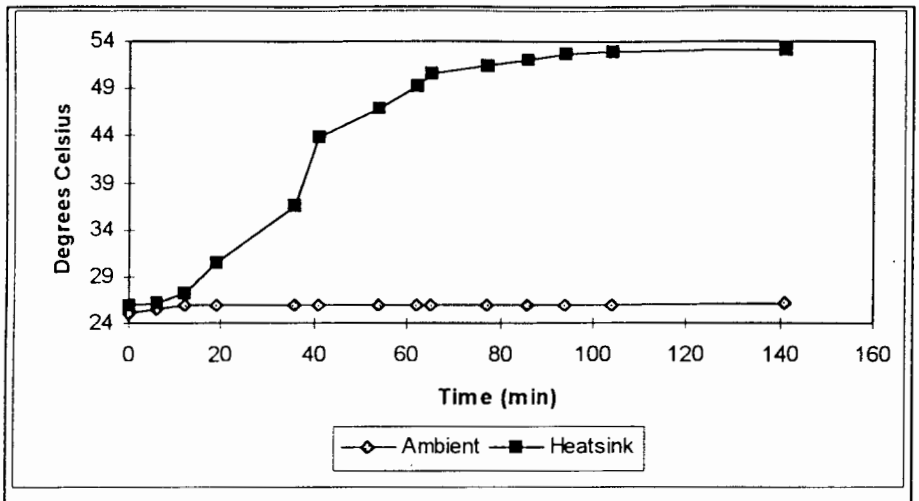

Figure 50: Heatsink thermal calibration - natural cooling

From Figure 50, the thermal resistance is found to be 0.28°C/W. This compares favourably with the manufacturer's $R_{\theta sa} = 0.27°C/W$.

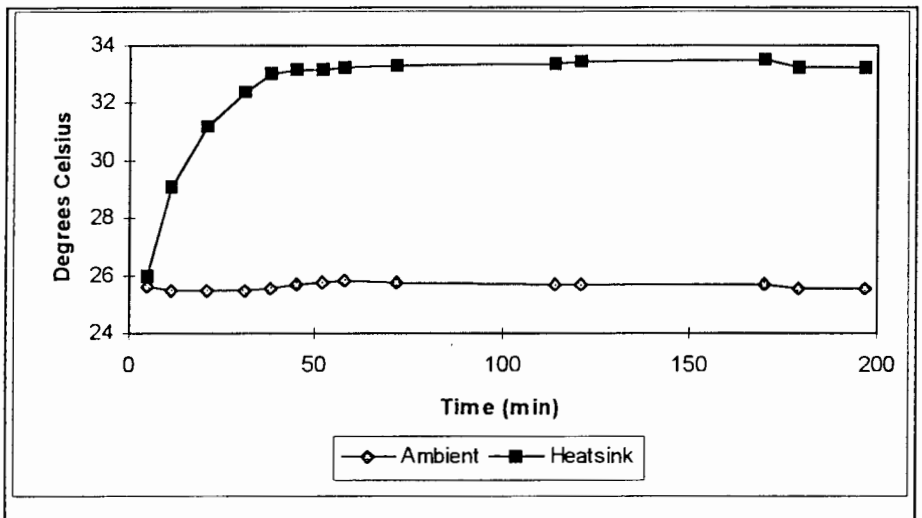

Figure 51: Heatsink thermal calibration - forced cooling

The effect of forced cooling is clearly visible in Figure 51. The maximum heatsink temperature is only 33.3°C versus the 53.8°C in Figure 50. This reduces the thermal resistance to $R_{\theta sa} = 0.076°C/W$, a 3:1 improvement over the natural cooled heatsink.

These results indicate that the heatsink and air-duct will ensure that the IGBT junction temperature does not exceed the desired $T_{j(max)} = 125°C$. However, the safety margin is only 0.003°C/W - less than $R_{\theta cs}$. If the assumption that the maximum UPS cabinet temperature of 45°C is incorrect, the IGBT modules could be destroyed by thermal runaway. This is possible since the switching losses of an IGBT are highly dependent on temperature. The increased cabinet temperature would in turn increase P_d which would in turn increase T_j and so increase P_d etc. With such a small margin, thermal runaway could also be induced by a change in altitude - the efficiency of a heatsink decreases with increased altitude. *The thermal design of the current system - because*

of the lack of a reasonable safety margin - is not robust. It is however considered sufficient for the prototype system.

In a UPS application, the reliability of the equipment is of utmost importance. Since the failure rate for semiconductor devices doubles for each 10°C increase above 50°C, the UPS thermal design should aim for an even lower $T_{j(max)}$. This could be accomplished by a larger heatsink or by increasing the air-volume forced through the duct per hour. Except for a water-cooled sink, it would be very difficult to keep the case temperature of the IGBTs at less than 90°C.

6.6 The construction of the power circuit

Before the IGBT modules were mounted, the heatsink was first machined to ensure a flush mounting. All mating surfaces were coated with a thin layer of thermal grease to ensure a good thermal conductivity. The thermal grease is used to remove the air from between the microscopic high points on the mating surfaces to effectively utilise the entire surface area for heat conduction. The IGBT modules were then fastened according to the manufacturer's torque specifications. All exposed areas of the heatsink were lacquered to prevent the aluminium oxidising, reducing its effectiveness to dissipate heat due to an increased thermal resistance.

To reduce the inductance, the DC bus was connected using two flat parallel copper bus-bars. The copper cross-section was calculated to ensure that no overheating of the IGBT is caused by bus-bar heating. The circuit inductance was further minimised by mounting the electrolytic bus capacitors symmetrically above the two IGBT blocks. To improve the high frequency response, each electrolytic was bypassed with a WIMA MKS-4 polyester film capacitor.

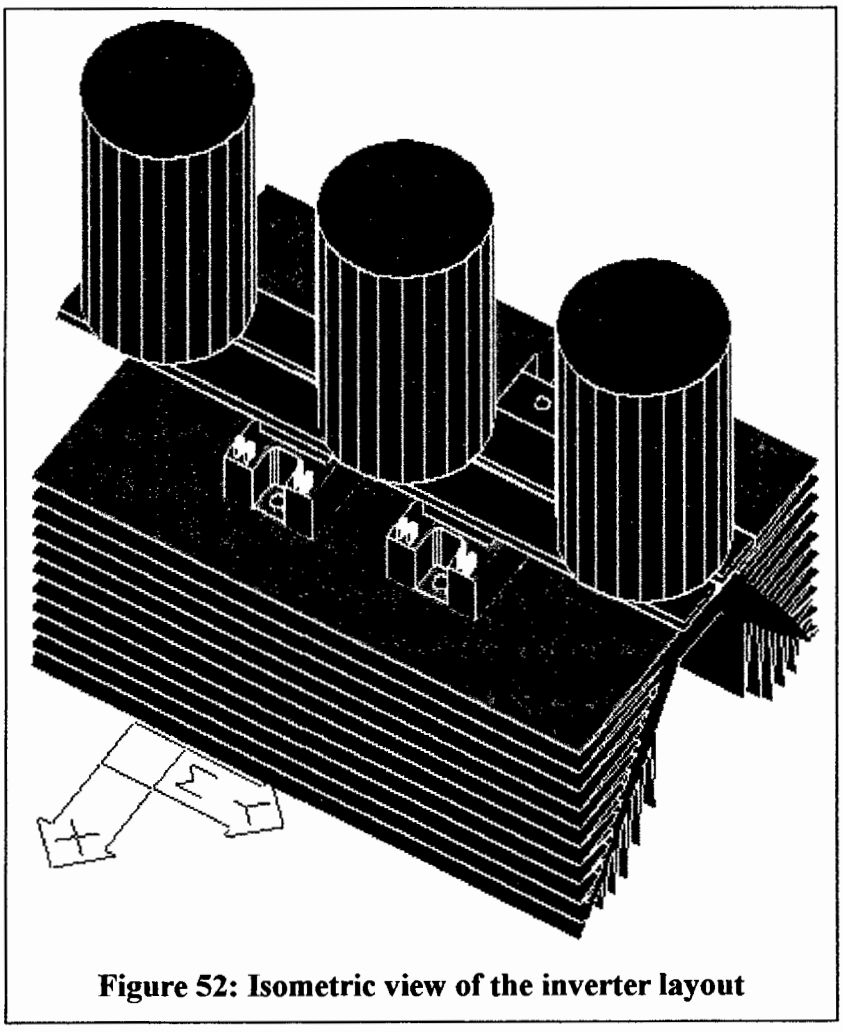

Figure 52: Isometric view of the inverter layout

Photographic images of the final converter construction are given in Appendix K.

7. Filter Design

This chapter describes the selection of the UPS input filter and the design of the inverter output filter.

7.1 Input Filter

EMI (Electromagnetic Interference) also known as RFI (Radio Frequency Interference), is unwanted electromagnetic energy that propagates via radiation and conduction over system signal and power lines. Conducted EMI can affect the operation of other electrical equipment connected to the same source[39]. Although EMI cannot be eliminated completely, it can be attenuated to safe levels as recommended by the Federal Communications Commission (FCC) and similar organisations.

An EMI filter used on the power line is a low pass filter that:

- Prevents the entry of high frequency interference carried by the AC power line into the protected equipment.
- Prevents the exit of interference energy generated within the protected equipment into the AC power line.

The basic approach to EMI filtering is to use a combination of inductors and capacitors to divert the flow of EMI currents away from the victim while at the same time allow the low frequency (50Hz) operating current to pass through unaffected.

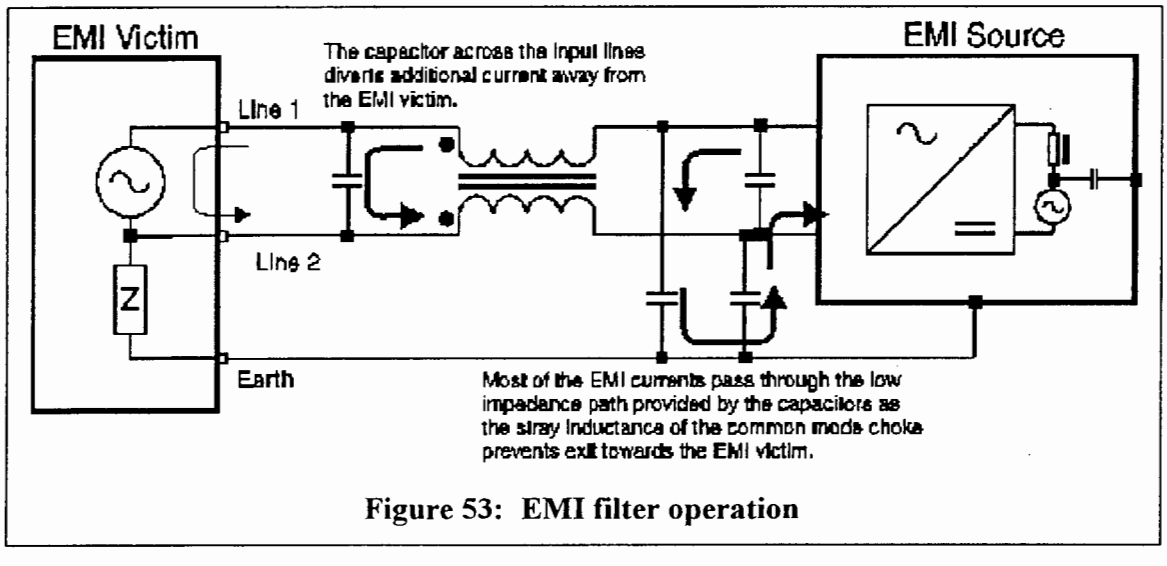

Figure 53: EMI filter operation

Referring to Figure 53. Filtering common mode EMI requires capacitors to earth. These capacitors are classified as Y capacitors and safety regulations limit these capacitors to relatively low values. Consequently, high values of inductance are

[39] EMC (Electromagnetic Compatibility) versus EMI is the ability of a system to function reliably in the presence of significant levels of EMI.

essential for effective filtering. Differential mode filtering requires capacitors across the input lines. These capacitors are classified as X capacitors.

Rather than design a new filter, an off-the-shelf FCC compliant EMI filter was selected with a sufficient current and voltage handling capability.

Effective reduction of interference requires proper installation of an EMI filter. Ideally, the EMI filter should be mounted at the point where the power line enters the UPS cabinet. As the prototype system not have a cabinet, the filter was mounted against the wall socket. To prevent the system radiating interference, all leads were twisted and wherever possible, shielded cabling was used.

7.2 Output Filter

The purpose of the output filter is to reduce the harmonic content of the inverter output to an acceptable level. Therefore the filter specifications are based on the inverter PWM harmonic spectrum. During the design and implementation of the filter, due consideration must also be given to the transient response of the output voltage i.e. when the load is suddenly connected or disconnected.

7.2.1 Specifications

The calculated harmonic spectrum for the inverter switching at 6.274kHz (m_f=125.5) with m_a=0.86 is given in Figure 54. An 8192-point FFT applied over a single output cycle of 20 milliseconds was used to generate the plot.

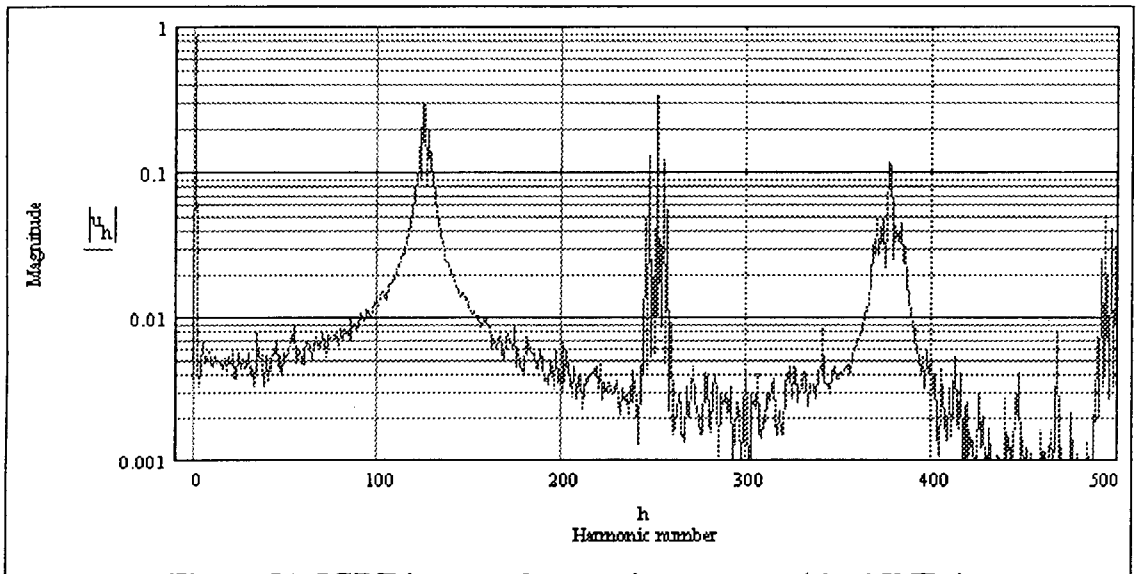

Figure 54: IGBT inverter harmonic spectrum (0 - 25kHz)

Including the first N/2 terms, the THD for the inverter output in Figure 54 is calculated as 94.4% . The output filter should ensure a THD of no more than 5%. To allow for a safety margin, a design THD of 4% was chosen.

The output filter, located between the inverter and load, must be designed to avoid interactions and instability not only with the load but also with the inverter output.

Interactions may be avoided if the design incorporates both the input and output impedance characteristics of the output filter.

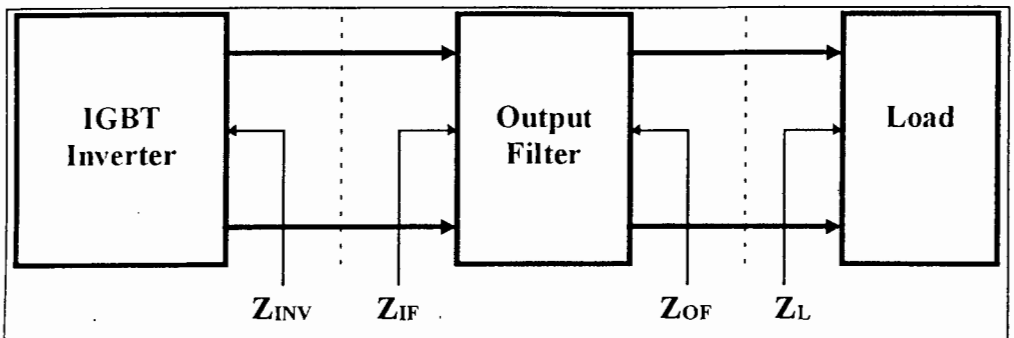

Figure 55: Output filter impedance specifications

The following filter impedance specifications must be satisfied (Figure 55).

$$|Z_{INV}| < |Z_{IF}|$$
$$|Z_{OF}| < |Z_{L}|$$

Besides providing the required attenuation, the output filter should also be designed with highest possible input impedance Z_{IF} while providing the lowest possible output impedance Z_{OF} to the load. It is important to note that these requirements are conflicting as both the input and output impedance are proportional to its characteristic impedance - a filter designed for a large input impedance has a large output impedance.

7.2.2 Configuration

Ideally the inverter filter should have a band-pass characteristic with the centre frequency tuned to 50 hertz. This would ensure a small current component in a parallel configuration or a minimal voltage drop across a series filter.

The components for a parallel band-pass LC-filter are unwieldy as they must be selected for the line frequency. A high-Q ($= \omega \cdot C \cdot R$) is also desirable to reduce losses and provide the required attenuation. A slight conduction imbalance between the upper and lower IGBTs, due to temperature or process variations will result in a large DC current through the inductor. This can however be prevented by actively adjusting the PWM but at the expense of an extra control loop. The centre frequency is also effected by the load impedance.

In a series LC-filter, the components are also selected for the line frequency. In addition, the capacitor must carry the rated load current. This requires a capacitor with a low ESR to prevent over-heating and possible failure.

An alternative is to use a low-pass LC-filter configuration (Figure 56).

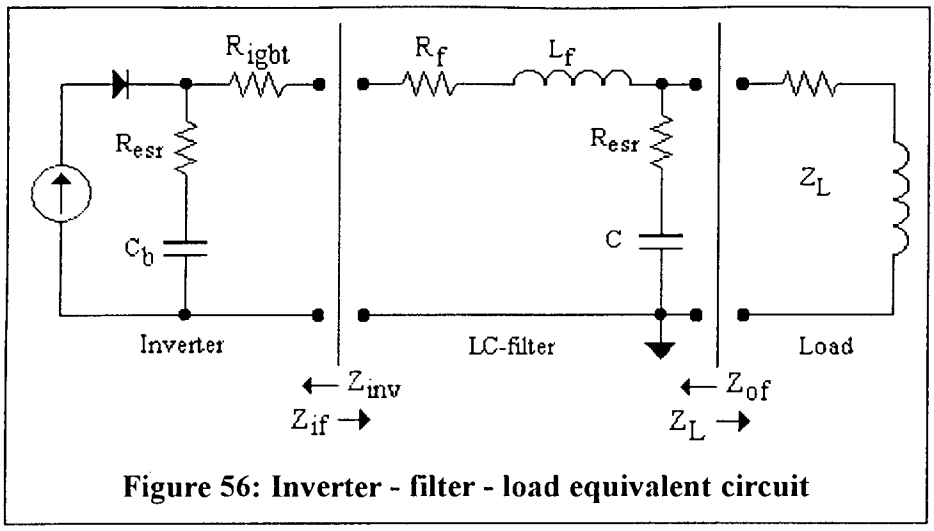

Figure 56: Inverter - filter - load equivalent circuit

With L=7mH and C=25uF, the following impedance relationships exist:

$$|Z_{INV}|_{f=50Hz} = 2.1 < \begin{bmatrix} |Z_{IF}|_{pf=0.5} = 22.8 \\ |Z_{IF}|_{pf=0.6} = 19.7 \\ |Z_{IF}|_{pf=0.7} = 17.8 \\ |Z_{IF}|_{pf=0.8} = 17 \\ |Z_{IF}|_{pf=0.9} = 18.5 \\ |Z_{IF}|_{pf=1} = 10.6 \end{bmatrix} \qquad |Z_{OF}|_{f=50Hz} = 1.03 < \begin{bmatrix} |Z_{L}|_{pf=0.5} = 21.2 \\ |Z_{L}|_{pf=0.6} = 17.6 \\ |Z_{L}|_{pf=0.7} = 15.1 \\ |Z_{L}|_{pf=0.8} = 13.2 \\ |Z_{L}|_{pf=0.9} = 11.8 \\ |Z_{L}|_{pf=1} = 10.6 \end{bmatrix}$$

As illustrated above, the design goals of avoiding interactions at both sides of the filter for various load power factors are met with the components selected. It can be shown that the output THD limit of 4% is also satisfied.

To reduce the transient recovery time, it necessary to use a 'light-weight' LC-filter which minimises the stored filter energy. Unfortunately 'light-weight' filters have inherently poor low-frequency harmonic attenuation characteristics. The harmonic purity of the output and transient performance are thus conflicting requirements. If either L or C in the current design is reduced to minimise energy storage, the THD limit is not satisfied.

7.2.3 Filter influence on the output voltage regulator

The transfer function for the filter-load combination is calculated as (14).

$$G(s) = \frac{1 + s \cdot C \cdot R_{esr}}{1 + s \cdot C \cdot \left(R_{esr} + R_f\right) + s^2 \cdot L_f \cdot C + \dfrac{1 + s \cdot C \cdot R_{esr}}{Z_L}} \qquad \ldots(14)$$

The zero in the filter response introduced by the capacitor ESR improves stability by increasing the phase margin. Unfortunately it also tends to exhibit large variations with temperature and manufacturing tolerances. Accordingly the output voltage regulator performance is optimised with minimal dependence on this parameter to guarantee loop stability under all conditions

The output filter also introduces a pair of complex poles. This peaking of the output filter near its resonant frequency may increase the overall loop gain above unity.

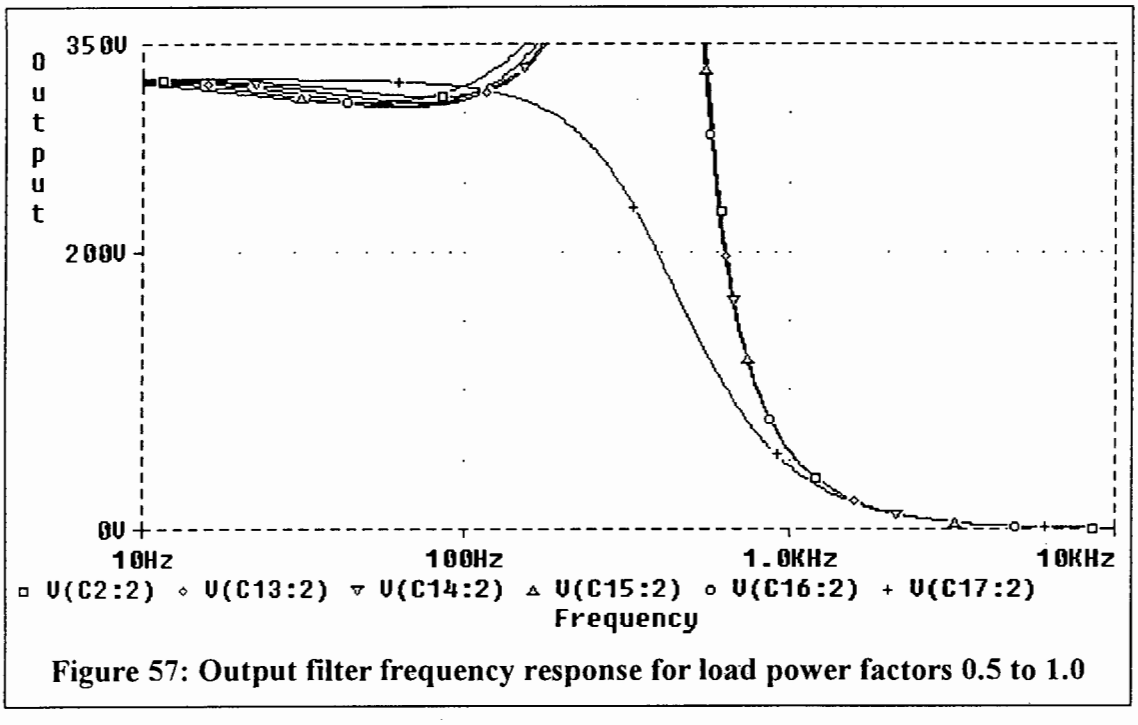

Figure 57: Output filter frequency response for load power factors 0.5 to 1.0

Figure 57 was generated using the PSpice simulation circuit depicted in Figure 58. Note the output impedance of the inverter is zero.

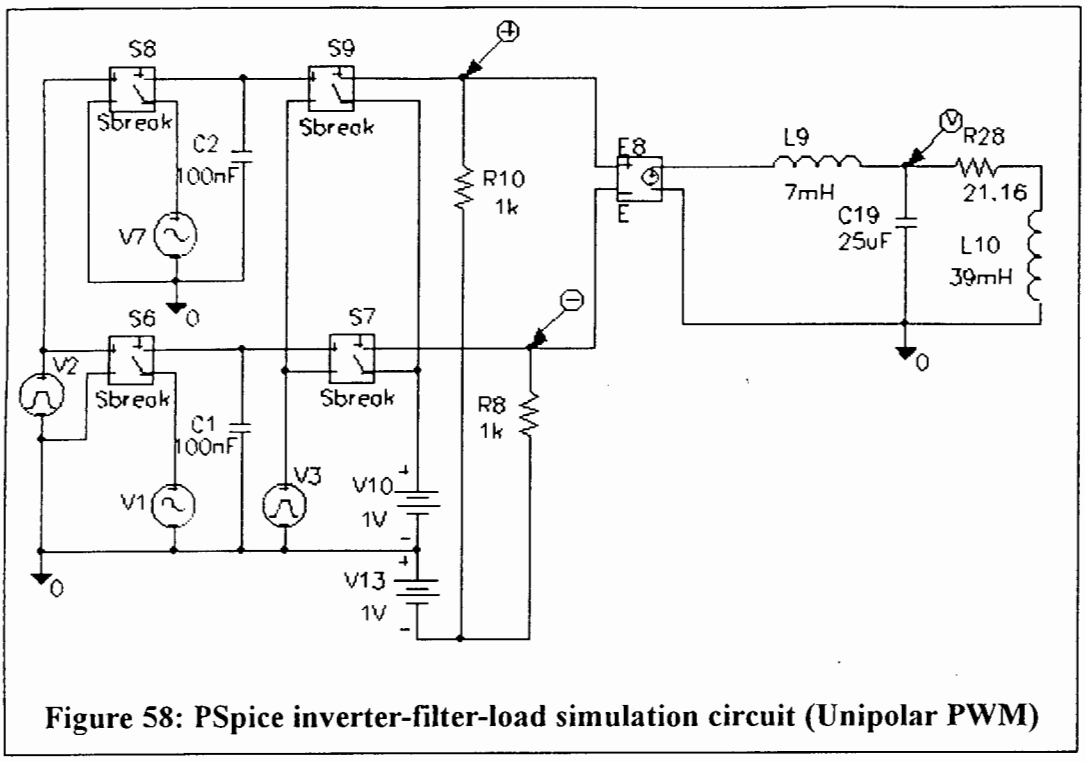

Figure 58: PSpice inverter-filter-load simulation circuit (Unipolar PWM)

8. Control software development

This chapter describes the control algorithms implemented within the UPS software. The "C" listing is given in Appendix F while the controller schematics are included in Appendix E.

8.1 Microcontroller selection

The Philips 80C552, a derivative of the popular MCS-51 microcontroller family was selected to control the UPS, as the development tools and experience were already available within the power electronics department. The block diagram of the 80C552 is given in Figure 59.

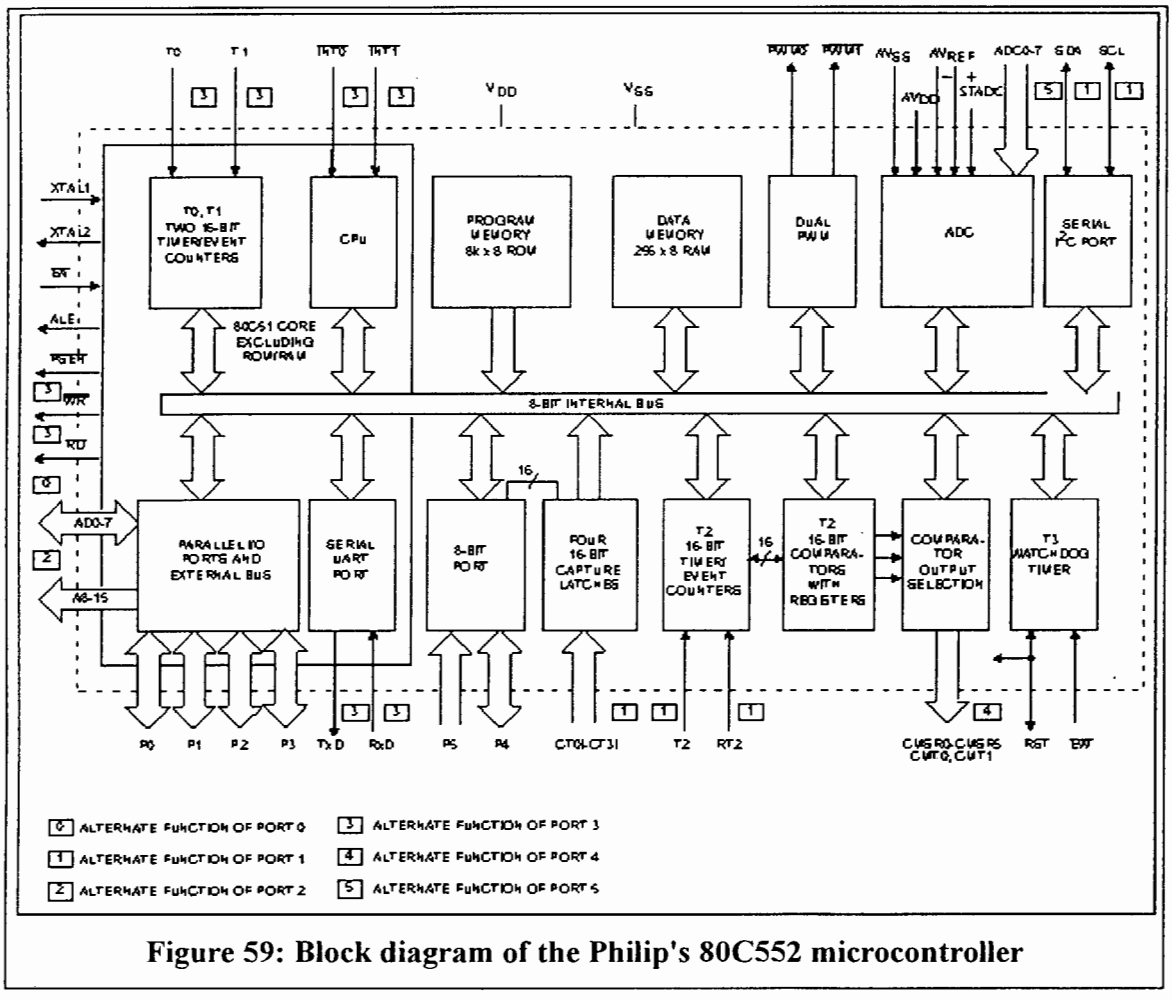

Figure 59: Block diagram of the Philip's 80C552 microcontroller

This derivative was selected primarily because of the dual PWM generators, 10-bit 8-channel analogue to digital converter and relatively high clock frequency of 16Mhz (instruction cycle time = 750 nanoseconds). For further information on the 80C552, consult the datasheet given in Appendix D.

8.1.1 Digital implementation considerations

Microcontroller-based control provides several benefits over traditional analog control methods e.g. the ability to implement sophisticated control algorithms which would normally have required complex hardware at high cost.

However, there are several implementation issues which must be considered:

- A/D conversion time and resolution - the former limits sampling frequency while the later is responsible for steady state errors and controller induced oscillations (limit cycles).
- PWM frequency and resolution. The time taken by the PWM module to change the duty cycle introduces a phase delay which is critical to the controller design as it limits the controller sampling rate and gain. A duty cycle update during a switching cycle may introduce glitches into the PWM output destabilising the controller.
- Computational delay - limits the controller complexity and performance.
- Word length and the effect on calculation precision.
- Sampling frequency - high sampling rates increase the processor burden but improves system performance. However, sampling above 40 times the system bandwidth yields diminishing returns[40].

8.1.2 Control signal interface

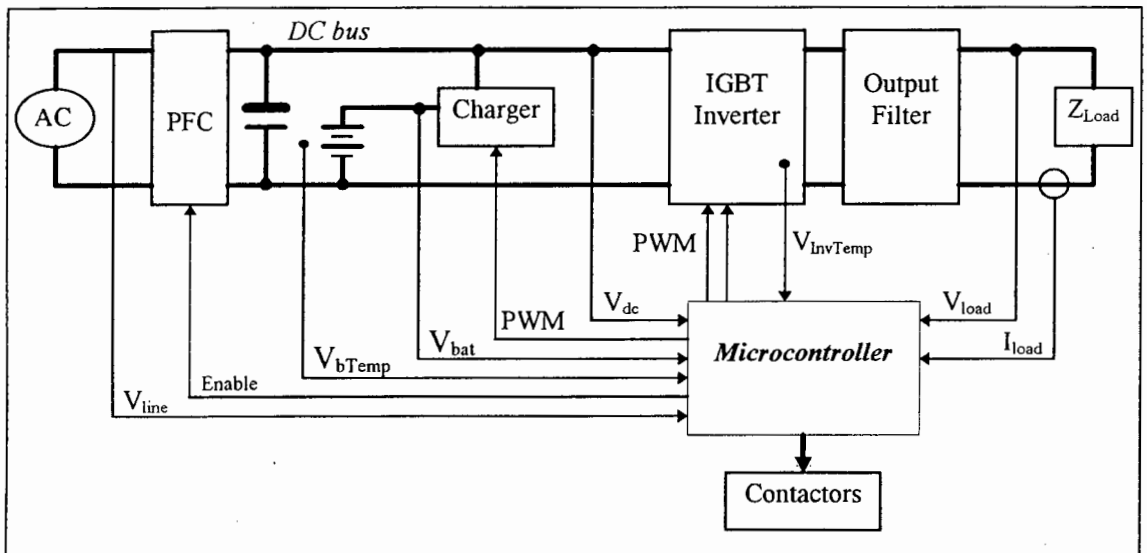

Figure 60: Control signal interface

The block diagram in Figure 60 outlines all the signals used and generated by the microcontroller. A detailed set of schematics is included in Appendix E. The process by which these signals are generated and processed follows.

[40] Franklin, GF.; Powell, JD.; Workman, ML.; "Digital Control of Dynamic Systems", 2nd Edition, Addison-Wesley, Massachusetts, 1990

8.2 Software flowchart

The software flowchart is given in Figure 61. All control algorithms are embedded within the main program, while the interrupt routines provide information to the main program or process the information generated by the main program. In either case, the information is transferred between the two software levels through a set of globally accessible data registers.

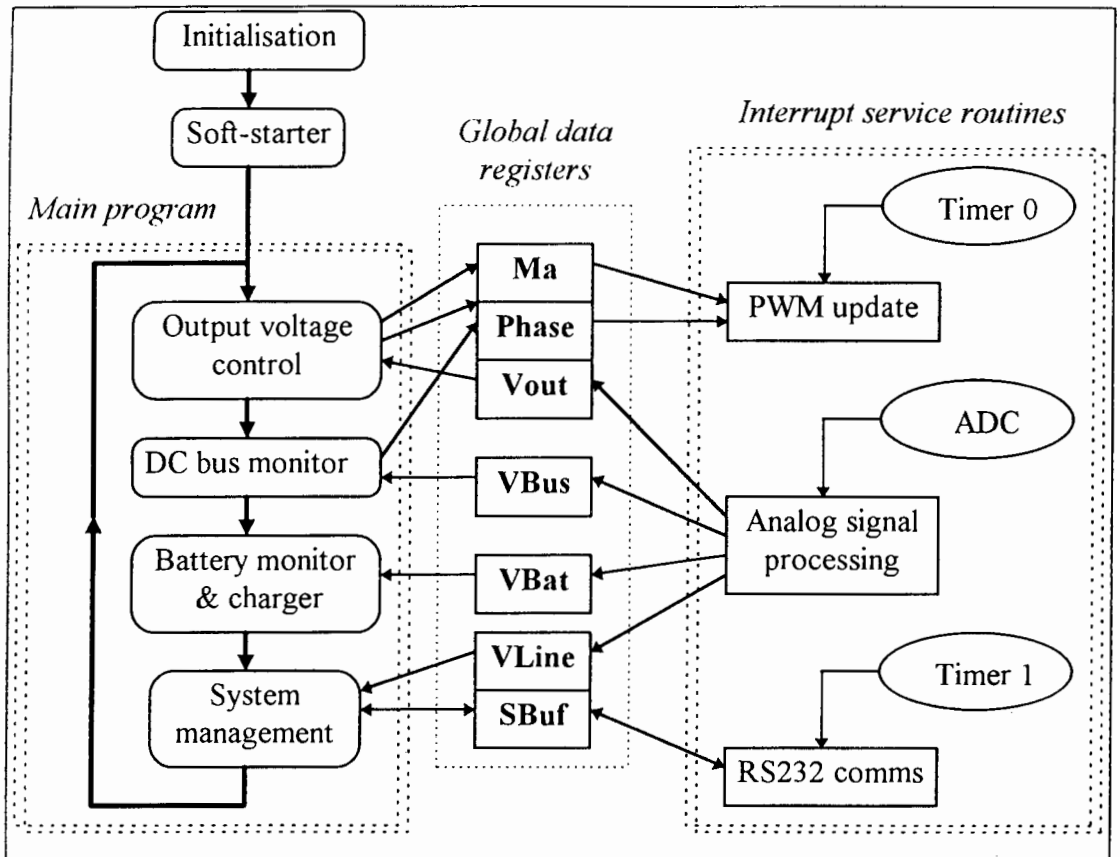

Figure 61: Controller software flowchart

For maintainability and portability, the majority of the software was written in "C". The source code was compiled to object format and linked into binary format using the KeilC51 development tools[41]. To speed the debugging process, the binary file was loaded into a Viper™ EPROM emulator[42]. Only once the code was operating as expected was an EPROM programmed and inserted into the controller board.

To assist the debugging process, a monitor program was developed to echo register values and data back to the PC through the serial communications port. The monitor code formed the basis for the Microsoft Windows-based UPS control panel, discussed in section 8.4.3.

[41] C51 V5.10, Keil ELEKTRONIK GmbH, 1995
[42] Viper 2, Bushy Inc. ,1995

8.3 Main control program

During initialisation, the controller performs a number of tests on the UPS hardware (program memory checksum, battery level, voltage and current feedback levels). The results of these tests are echoed through the RS232 communications channel.

Thereafter, the processor loops sequentially through the current and voltage controller, DC bus monitor, ripple regulator, battery charger and system management code.

8.3.1 Current controller

Arbitrary loads cannot be fed directly as any imbalance between the upper and lower switching elements of the inverter will result in a DC component.

The presence of DC in a transformer-like load can saturate the core material due to the asymmetric transversal of the B-H curve. The subsequent loss of impedance and resulting over-currents will most probably damage the load, inverter or both.

The general solution is an isolation transformer attached to the inverter output with a small air-gap and low flux density. An alternative, as adopted in the current system, is to nullify the DC component through actively adjusting the inverter gate drive signals.

The same current control loop is also used for detecting over-loads and short-circuit conditions.

8.3.2 Voltage controller

The purpose of the voltage controller is to minimise the inverters output impedance. Since the selected microcontroller has a limited arithmetic ability, the control algorithm must be carefully selected. A compromise between performance and control complexity is therefore necessary.

A simple strategy such as proportional-integral (PI) control based on integer calculations is easy to implement and achieves high sample rates. However the performance will suffer due to the simplicity of the control. A complex strategy such as adaptive non-linear control will incur longer calculation times. The resultant lower sampling rate degrades performance.

A proportional-integral-derivative (PID) controller was selected as it is relatively straightforward to implement and allows various trade-offs to minimise calculation times.

The continuous time transfer function of a PID controller is given by (15).

$$K(s) = K_P + {}^{K_I}\!/_{s} + K_D \cdot s \qquad \ldots(15)$$

Converting (15) from the Laplace domain into the digital z-domain using the bilinear transform yields,

$$D(z) = \frac{(2 \cdot K_P \cdot T + K_I \cdot T^2 + 2 \cdot K_D) \cdot z^2 + (K_I \cdot T^2 - 2 \cdot K_P \cdot T - 4 \cdot K_D) \cdot z + 2 \cdot K_D}{2 \cdot T \cdot z \cdot (z-1)} \quad ...(16)$$

where T is the sampling period.

Thus the digital PID controller has an insignificant pole at $z = 0$ and a dominant pole at $z = 1$. Roots that are near the origin of the z-plane are the least significant since $s \to -\infty, z \to 0$. There are also two zeros which can be either real or complex. With error e[n] and plant input u[n], calculating the difference equation yields,

$$u[n] = u[n-1] + K_1 \cdot e[n] + K_2 \cdot e[n-1] + \frac{K_D}{T} \cdot e[n-2] \quad ...(17)$$

where

$$e[n] = Setpoint - y[n]$$

$$K_1 = \frac{2 \cdot K_P \cdot T + K_I \cdot T^2 + 2 \cdot K_D}{2 \cdot T}$$

and

$$K_2 = \frac{K_I \cdot T^2 - 2 \cdot K_P \cdot T - 4 \cdot K_D}{2 \cdot T}$$

From (17) it is noted that three multiplication's and four addition / subtractions are required before the duty cycle can be updated (assuming the coefficients are calculated off-line). For a floating-point evaluation, 2300 processor cycles are required while an integer approximation will consume at least 408 cycles. The former implies an absolute maximum of 13 control calculations per 50Hz cycle. Besides reducing the controller complexity, the later option is the only viable alternative.

The voltage control system is illustrated in Figure 62. Since the load is arbitrary, it is modelled as a disturbance to the control loop. From the output voltage y[n] and admittance $Y = G + j \cdot B$, the load current is evaluated. The disturbance, calculated from the inverter impedance and load current, is then subtracted from the output voltage. A sudden change in the load is simulated by multiplying the load current by a step-waveform (default = 1).

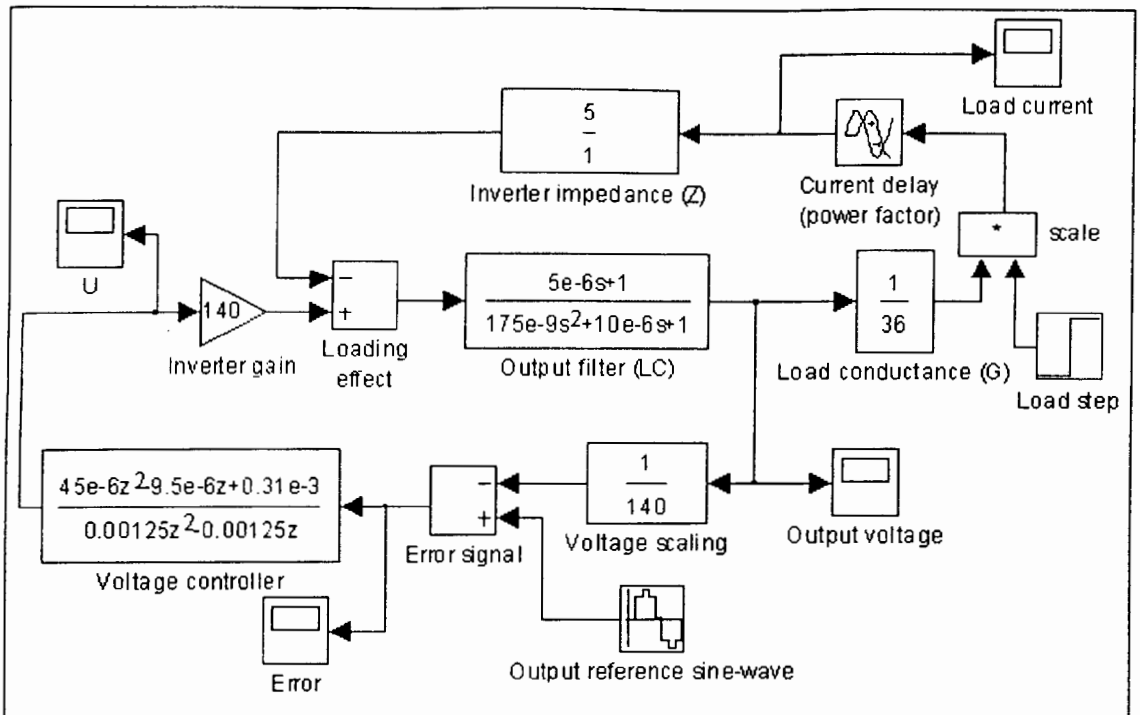

Figure 62: Voltage controller simulation using MATLAB's Simulink Toolbox

The controller controls the output voltage by modifying the unipolar PWM being fed to the inverter IGBTs. Two methods of adjusting the output voltage were investigated.

8.3.2.1 Voltage adjustment by phase-shifting the inverter legs

In a unipolar PWM driven inverter bridge, the first phase arm is modulated by:

$$Y_1(t) = M \cdot \sin(\omega \cdot t) \quad ...(18)$$

While the second phase arm is modulated by:

$$Y_2(t) = M \cdot \sin(\omega \cdot t - \alpha) \quad ...(19)$$

If $\alpha = \pi$, as is the usual case, the fundamental output of the inverter is given by:

$$Y_0(t) = Y_1(t) - Y_2(t) = 2 \cdot M \cdot \sin(\omega \cdot t) \quad ...(20)$$

However, assuming $\alpha = \lambda$ and $0 < \lambda < \pi$, then it can be shown that the output is given by:

$$Y_0(t,\lambda) = M \cdot \sqrt{2 \cdot (1 - \cos\lambda)} \cdot \sin\left(\omega \cdot t - a\tan\left(\cot\frac{\lambda}{2}\right)\right) = M_a(\lambda) \cdot \sin(\omega \cdot t - \beta)$$

...(21)

From (21), it can be seen that the output amplitude can be adjusted by simply changing the phase between the inverter legs. The adjustment does however shift the output

voltage by β degrees. Fortunately this shift is easily corrected by a -β shift of the output index.

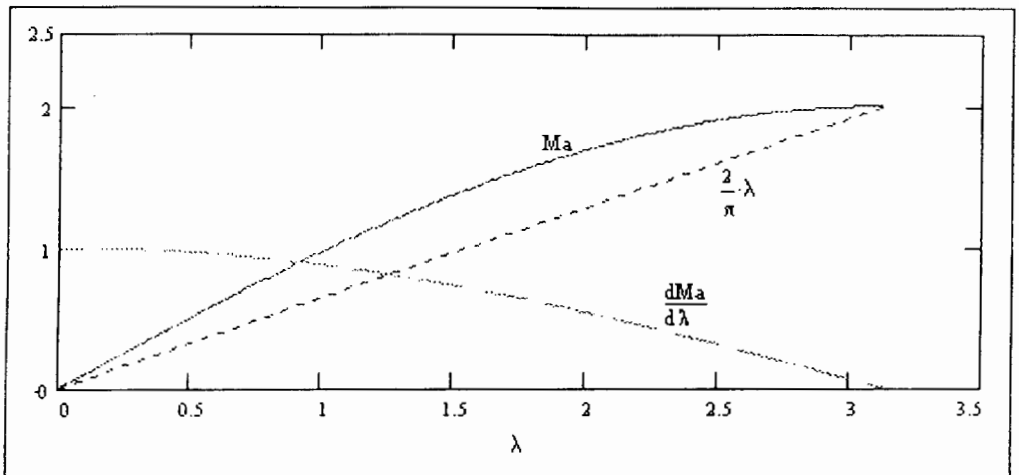

Figure 63: Output voltage magnitude as a function of the phase shift λ

The magnitude of (21) and derivative given by (22) are plotted in Figure 63.

$$\frac{d}{d\lambda} M_a(\lambda) = \frac{M}{\sqrt{2 \cdot (1 - \cos\lambda)}} \cdot \sin\lambda \qquad ...(22)$$

As the DC bus voltage falls under load or during the transfer to the battery pack, the voltage controller will increase λ in order to maintain the output voltage. From (22) it is noted that as the phase shift λ between the inverter legs approaches π, the output voltage resolution increases. This effect complicates the design of output controller as the Δλ required to bring about the same correction in the output voltage must be linked to the derivative.

Although the software required to implement the above voltage adjustment is ideal for an 8-bit microcontroller (Appendix G), the complications to voltage controller resulted in the following method being implemented on the UPS system.

8.3.2.2 Voltage adjustment by pulse scaling

This is the direct method of controlling the output voltage. Each pulse is multiplied by a modulation factor M_a, where $0 \leq M_a \leq 1$[43]. The fundamental output of the inverter is then given by (23).

$$Y_0(t) = Y_1(t) - Y_2(t) = M_a \cdot V_{DC(bus)} \cdot \sin(\omega \cdot t) \qquad ...(23)$$

[43] In regular sampled sinusoidal PWM, the modulation range can be extended by adding a zero-sequence component - see Bowes, SR.; Lai, YS.; "The relationship between space-vector modulation and regular-sampled PWM", IEEE TIA, Vol. 44, No. 5, October 1997

The output resolution, assuming a maximum DC bus voltage of 400V is 2.745V. With this level of control, the required $230V_{RMS}$ output can be adjusted within 1%. The code implementing (23) on the microcontroller is included in the main software listing.

8.3.3 DC bus monitor

The DC bus monitor is used to detect a supply failure. During a failure, the PFC is unable to maintain the DC bus voltage. Once the voltage has fallen sufficiently, the monitor enables the battery pack. The PFC continues operation, but is supplied from the battery pack until it is exhausted or the supply returns.

During a line swell or sudden loss of load, the monitor will disable the PFC. This is to prevent over stressing the electrolytic capacitors. The bleeder resistors provide the second level of defence against over-voltage.

8.3.4 Ripple regulator

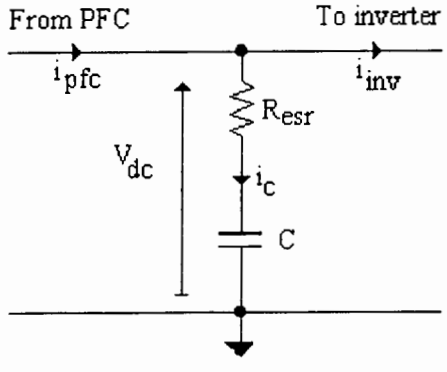

Figure 64: Ripple calculation circuit

Ignoring the high frequency components, the PFC delivers a current into the bus capacitor C given by (24).

$$i_{pfc}(t) = K \cdot |\sin(\omega \cdot t)| \quad ...(24)$$

Similarly, assuming a resistive load, the IGBT inverter extracts a current given by (25).

$$i_{inv}(t) = K \cdot |\sin(\omega \cdot t + \phi)| \quad ...(25)$$

The resultant current $i_c(t)$ contributes to the ripple voltage across the capacitor C.

$$V_r(t) = \frac{1}{C} \cdot \int_t^{t+T} (i_{pfc}(t) - i_{inv}(t)) \cdot dt \quad ...(26)$$

By adjusting the phase angle ϕ of the inverter, the resultant current and therefore voltage ripple is minimised. This reduces the DC bus losses given by (27), improves system efficiency and increases the MTBF (lower temperature cycling).

$$P_{loss(C)} = i_c^2 \cdot R_{esr} \quad ...(27)$$

By synchronising the currents, the required bus capacitance is reduced.

The effect of phase-shifting on the DC bus ripple is illustrated in Figure 65. Initially the inverter current is 180 degrees out-of-phase with the PFC current. This difference results in a very large voltage ripple. The bus monitor manages to reduce this ripple by

more than 80% within 60 seconds. It then maintains this reduced ripple voltage until the load changes.

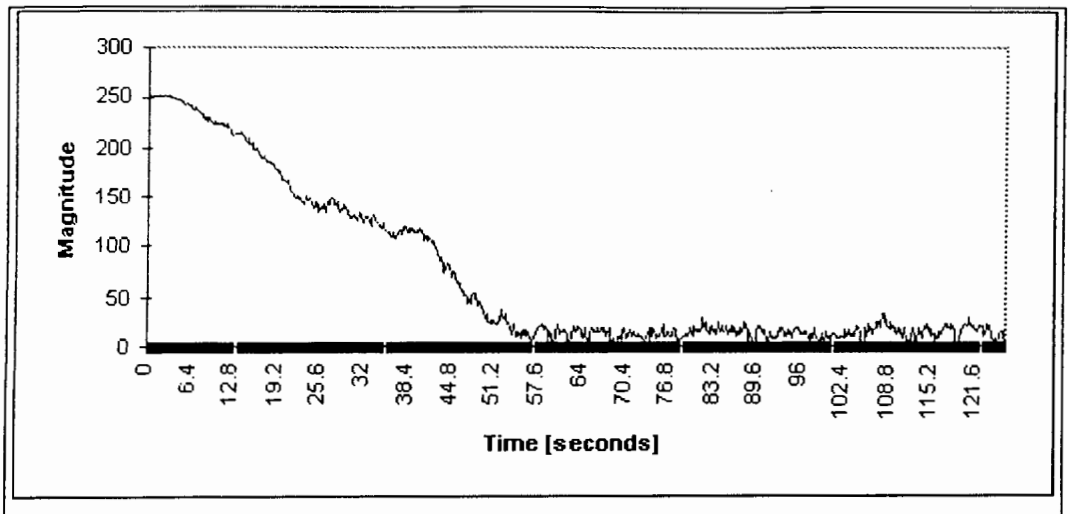

Figure 65: Reduction of the DC ripple by phase-shifting the inverter output

The ripple magnitude can be reduced sooner using smaller time constants, but at the expense of greater noise susceptibility and possible oscillation. As the load connected to a UPS is usually fairly constant, a fast response is not necessary. The rate at which the inverter phase is adjusted must however be limited so as not to adversely effect the load.

The effect of a reactive load on the DC bus ripple regulator is analysed in Appendix I.

8.3.5 Battery monitor and charger

The task of the battery monitor and charger is to maximise capacity and extend operational life of the series connected battery pack.

The charger code monitors and controls both charging voltage and charging current through three separate states: (1) a high current bulk-charge state, (2) a controlled over-charge and (3) a float or standby state (Figure 66).

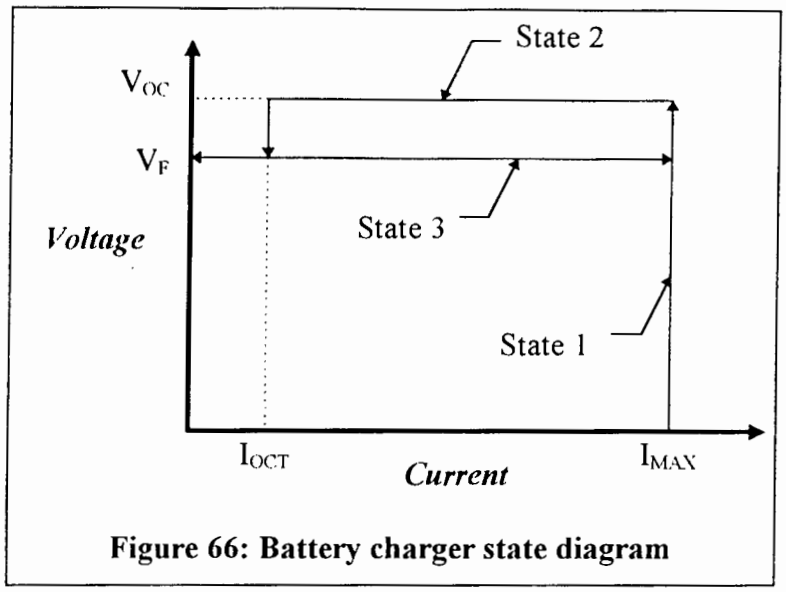

Figure 66: Battery charger state diagram

In the bulk charge state, the charger acts like a current source providing a maximum current of I_{MAX} until the battery voltage has reached V_{OC}. This state returns approximately 70% of the capacity back to the battery. During the over-charge cycle, the charger regulates the battery voltage at an elevated level of V_{OC} until the charging current has dropped to I_{OCT}. In the final state, the charger drops the voltage to the float level of V_F and maintains this level. The float level is used to compensate for self-discharge of the battery pack.

Feedback from a temperature probe was used to compensate for the negative temperature dependence of the voltage characteristic i.e. -4mV/°C per 2V cell.

8.3.6 System management

The main task of the system management code is to ensure the UPS operates within its specifications.

To limit the inrush current during power-up, the system code charges the DC bus through a resistor. Once the bus voltage is sufficient, the resistor is bypassed by a relay, the power factor corrector is then enabled, followed by the inverter. The system manager software then begins monitoring the voltages, load current and heat-sink temperatures.

If the inverter must be bypassed (over-temperature, over-load or maintenance), the system manager disables the bus monitor and enables a digital phase-locked loop (DPLL). The DPLL is used to synchronise the incoming supply voltage with the inverter output voltage. The voltages are always shifted unless the load has a unity power factor. Once synchronised, the DPLL enables a mechanical bypass relay 5 to 6 milliseconds before the load zero-current crossing. As the relay contactors make contact at the zero-crossing, minimising arcing and the generation of EMI, the DPLL disables the IGBT inverter.

8.4 Interrupt service routines

For maximum speed, all the interrupt service routines were coded and optimised in assembly.

8.4.1 Inverter PWM update

The unipolar PWM update routine is called continuously at a rate equal to the switching frequency. The update processing is divided into two sections, namely: output frequency generation and pulse calculation.

8.4.1.1 Output frequency generation

To synthesise the 50 hertz output frequency, a technique known as direct digital synthesis (DDS) was employed. In DDS, a counter known as a phase accumulator is used to track the output waveform phase angle. The counter also serves as the index for the PWM sine-wave look-up table. During each interrupt call, the phase accumulator is incremented by the amount stored in the phase increment register. Since the phase increment register can contain any arbitrary value, including fractional parts, sine-waves of variable frequency can be synthesised.

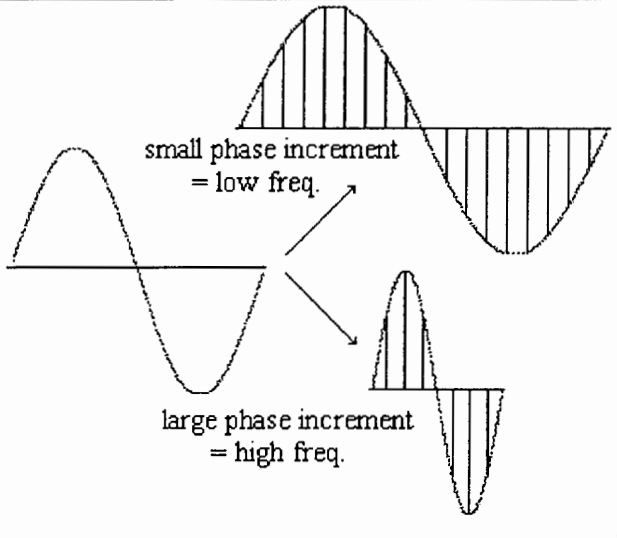

Figure 67: Output waveform generation using the DDS technique

To implement the DDS technique on the microcontroller, 16-bit registers are used for both the phase accumulator and phase increment registers. The phase increment value is then calculated from (28).

$$PhaseInc = \frac{f_m \cdot 2^n}{f_{switch}} = \frac{50 \cdot 65536}{6274.51} \cong 522 \quad ...(28)$$

Due to hardware limitations, the output frequency generated is not exactly 50Hz but rather 49.98Hz. This discrepancy is not regarded as significant as very little mains powered equipment will be adversely affected by a -0.05% change in line frequency. If necessary, the accuracy of the output may be improved by increasing the number of bits used for the phase accumulator and phase increment registers.

8.4.1.2 Pulse calculation

The second stage of the interrupt routine is the update of the two 8-bit PWM channels. Each PWM channel can generate pulses of variable length and frequency. The

switching frequency f_s is programmed only once during initialisation using the *PWMP* register. The value loaded into *PWMP* is calculated from (29), where f_{osc}=16MHz.

$$PWMP = \frac{f_{osc}}{510 \cdot f_s} - 1 \qquad \ldots(29)$$

The output pulse width is controlled by modifying the *PWM0* and *PWM1* registers for the first and second inverter leg respectively. Sinusoidal PWM is generated by using the phase accumulator to index a sine table stored in the EPROM. The table value is read, scaled by M_a and then transferred into *PWM0*. *PWM1* is calculated by advancing the table index by 180 degrees. As a result, the widths of the pulses are proportional to the amplitude of the modulating sine wave at uniformly spaced sampling times T_s - hence the terminology 'uniform' or 'regular sampled' PWM.

In the current PWM system, only the falling edge is modulated. The effect of asymmetric modulation on the output harmonic spectrum is described in Appendix A.

8.4.2 Analogue to digital conversion

The analogue to digital interrupt service routine digitises the analogue signals presented on port 5 and stores the results in the processor internal data memory. Because the ADC is limited by a [0..5V] input range, all AC signals are first scaled and then level-shifted to 2.5V.

8.4.3 RS232 communications

A protocol is vital to the system's operation; it determines the method that the master and slave devices use to establish and break off communication; how the sender and receiver are identified; how messages are exchanged in an orderly manner and the way in which communications errors are detected.

Rather than develop a new protocol, the industry-standard Modicon protocol was implemented. The protocol defines a packet with a header byte followed by a flag or command byte, a number of data bytes and finally a 16-bit checksum. A detailed description of the protocol can be found in the "Gould Electronics Modicon Reference Guide"[44].

The data transferred to the PC is used by the UPS control panel to display the current status of the system (Figure 68). The finer operation details of are handled by a configuration panel (Figure 69). The data update rate was limited to 0.5 seconds so as not to overload the microcontroller.

[44] Internet web site: http:\\www.modicon.com

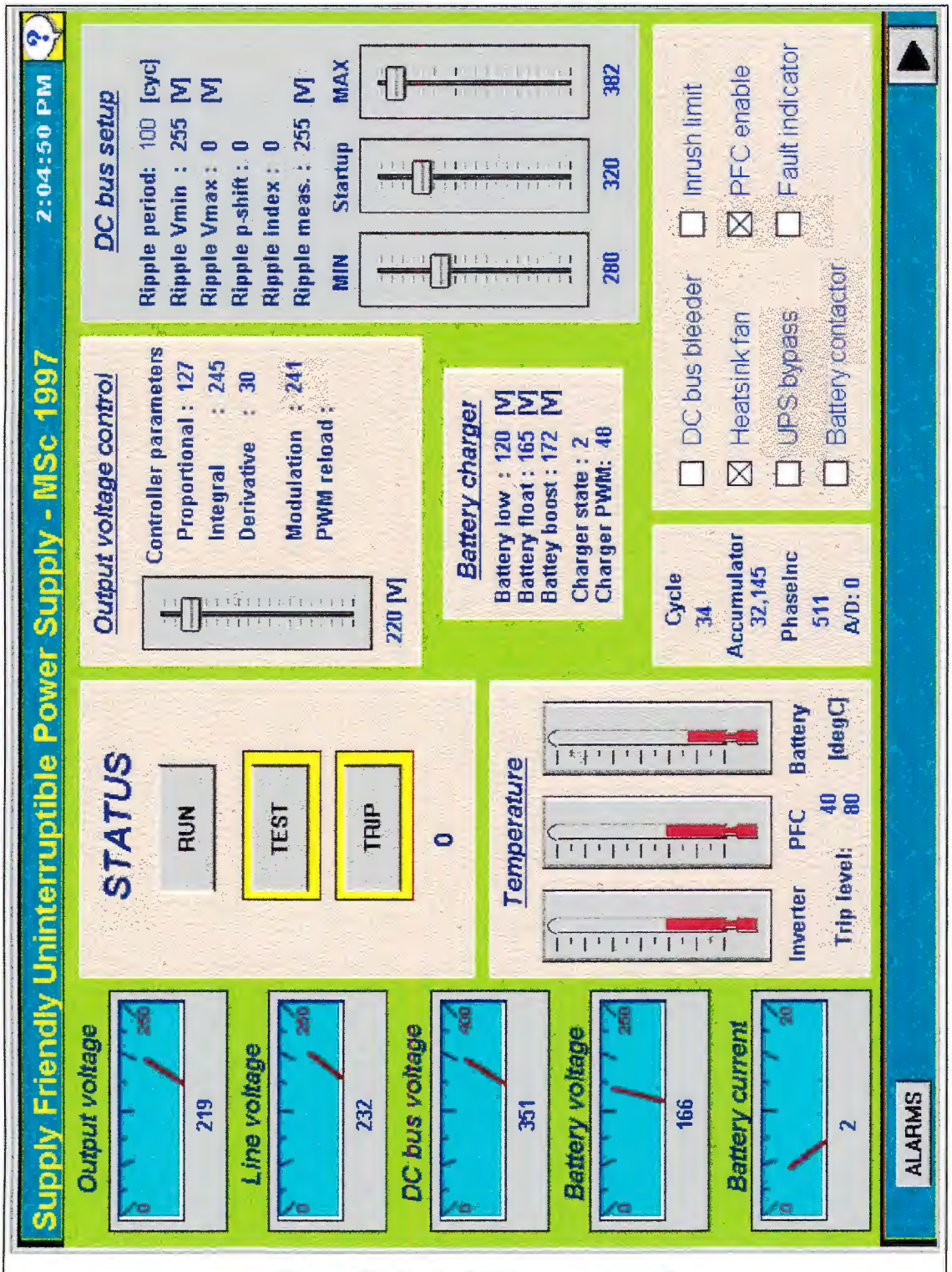

Figure 68: Main UPS control panel

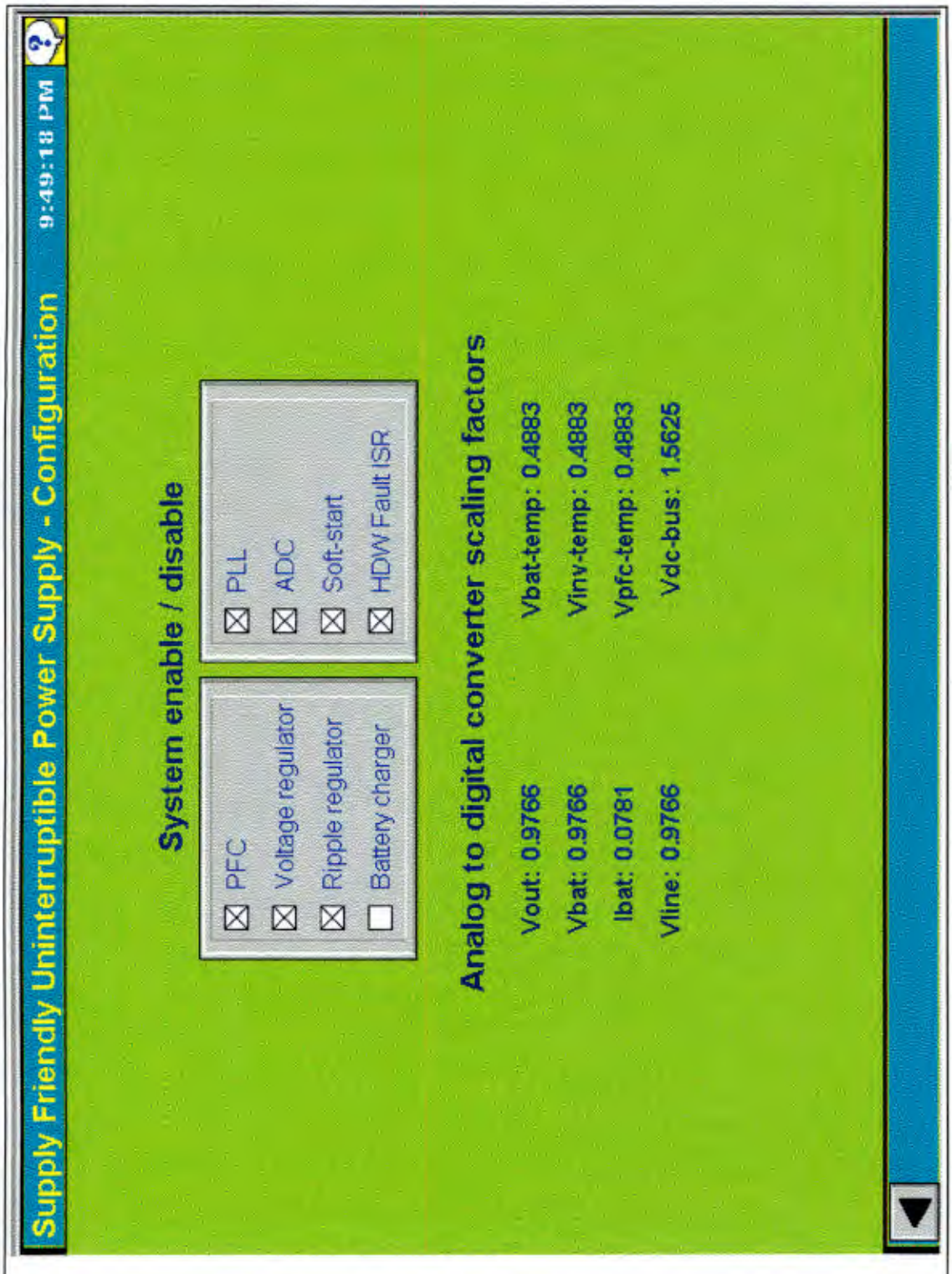

Figure 69: UPS configuration panel

From the control panel, the user is able to interrogate the system e.g. simulate power failures, bypass and diagnose system faults. The data is stored on the local PC hard-disk to facilitate maintenance and problem solving.

9. Performance Analysis

In this section, the performances of the PFC and single phase full-bridge inverter are evaluated. The results obtained are verified against the theoretical and the discrepancies explained.

9.1 Power factor corrector

9.1.1 Experimental set-up

A single-phase variac, driven through an isolation transformer, was used to adjust the line voltage delivered to the power factor corrector. A 15 amp circuit breaker provided an over-current trip. All waveforms and harmonic analyses were captured and performed using a Tektronix A622 current probe and THS720P hand-held digital oscilloscope[45].

9.1.2 Commissioning the PFC system

To commission the power factor corrector, a 300Ω (≈500W) resistive load was attached directly across the DC bus. The line voltage was then gently increased while monitoring the line current and MOSFET drain-source voltage.

As the load current increased, an audible sound emanating from the core increased. This phenomenon is attributed to magnetostriction[46]. As the core material is magnetised, it experiences a slight change in dimensions. Usually this is of no concern as converters operate above audible frequencies (>20kHz). However besides the 100kHz switching, the current application has a significant 100Hz component.

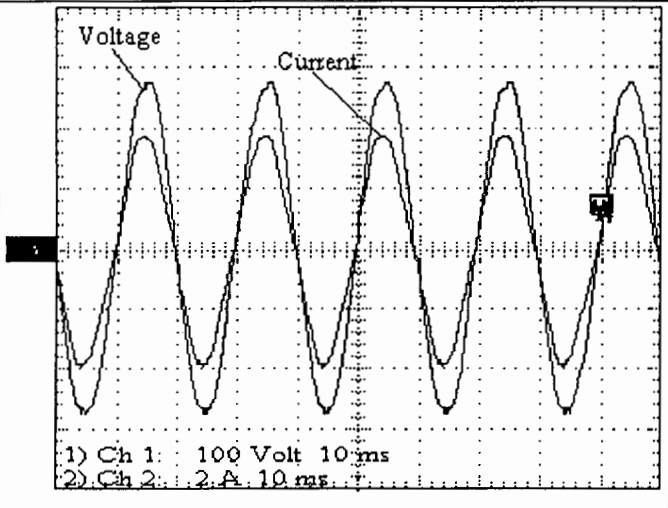

Figure 70: Line voltage and current at 500W

Displayed in Figure 70 is the line current for a line voltage of 195V. As indicated the current is sinusoidal and in phase with the voltage. The no-load DC bus voltage was 389V while under load the controller maintained the output at 386V for a line voltage sweep from 180V through to 250Vrms.

Harmonic analysis performed on the first 50 components of the voltage waveform revealed a total harmonic distortion (THD)

[45] The THS720P channels are electrically isolated from one another which facilitates power and harmonic measurements.

[46] Christiansen,D.; "Electronics Engineers' Handbook", 4th Edition, pp. 9.39-9.40, McGraw-Hill, 1996

of 2.96%. This was carried through the PFC multiplier and reflected by the 6.59% distortion of the line current. The PFC modulation process contributes 3.63%, well below the 5% design specification. This also indicates the advantage of using a pure sine-wave lookup table instead of the actual line voltage as a reference when attempting to minimise the current THD[47].

Further examination of the MOSFET drain-source voltage revealed a turn-on time of 161ns and turn-off of 386ns. The primary reason for the difference is the inability of the totem pole output stage of the UC3854 to rapidly charge / discharge the gate capacitance associated with a large power MOSFET. This drawback is readily overcome by the insertion of a PNP speed-up network between the UC3854 output and APT5012 gate as shown in Figure 71.

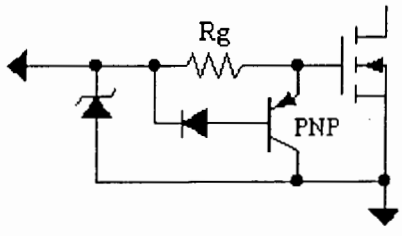

Figure 71: PNP speed-up network

When the IC initiates turn-off, the PNP epitaxial high speed transistor conducts hard, quickly discharging the MOSFET gate capacitance. The diode connected to the base is necessary to prevent the avalanching of the transistor base-emitter junction during turn-on. With the speed-up network installed, the turn-off time is reduced form 386ns to 127ns (see Figure 72) while the turn-on remains basically unchanged. Although the turn-on is not directly improved, there is a decrease in the peak diode recovery current. This is due to the reduced junction temperature resulting from the lower turn-off loss.

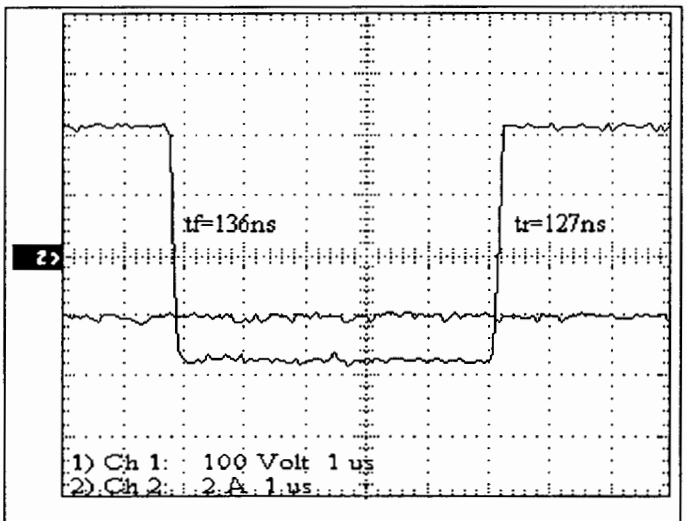

Figure 72: MOSFET drain-source voltage during turn-on and turn-off

Minimising stray inductance through careful component layout and the use of planar conductors results in very little overshoot and ringing on the MOSFET drain-source voltage as illustrated by Figure 72. However the inclusion of a high gain PNP transistor

[47] Merfret, I.; "Analysis and Application of a New Control Method for Continuous-mode boost Converters in Power Factor Correction Circuits", PESC 1997

has amplified the stray inductance in the gate drive circuit and resulted in the oscillatory response given by Figure 73. These high frequency oscillations ($T = 130ns \rightarrow 7.6MHz$) are radiated and readily detected by a spectrum analyser with an EMI / RFI probe.

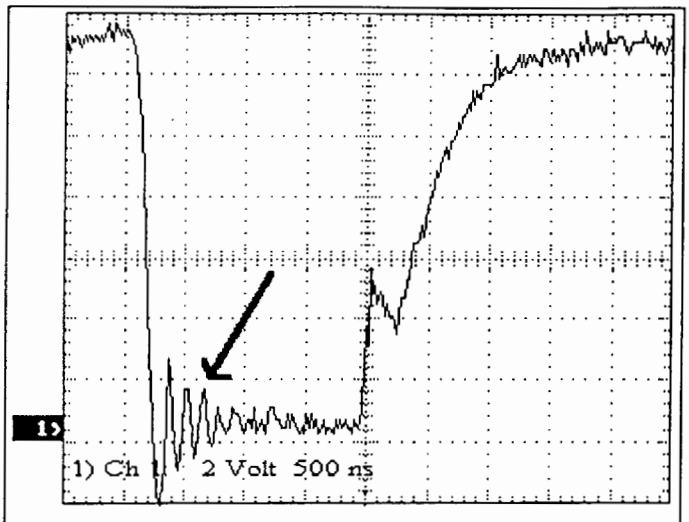

Figure 73: MOSFET gate voltage with the PNP speed-up network included

The delivery of a sinusoidal current into the DC bus capacitor results in a second harmonic ripple voltage as depicted by Figure 74.

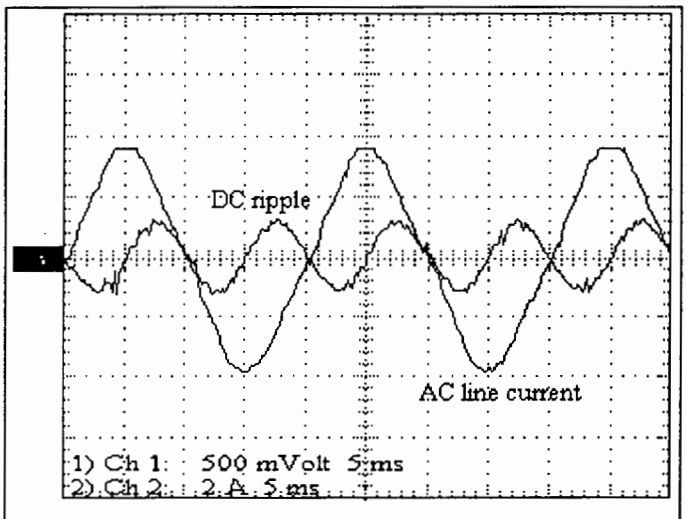

Figure 74: DC bus ripple versus line current

A two pole filter is used to attenuate this ripple before passing it through the multiplier - thereby minimising the distortion of the input current. A single pole filter with a low cut-off frequency serves the same purpose, however a two pole has a faster transient response for the same level of attenuation. The 180 degree phase shift also shifts the second harmonic back in phase with the voltage.

9.1.3 Efficiency analysis

To establish the efficiency, the PFC was operated at various power levels between 500W and 3000W. The high power variable load was constructed from a tank containing a copper-sulphate solution. The load adjustment was made by varying the electrode surface area. Each change in the output power level was accompanied by a waiting period (≈10 minutes) during which time the boost diode and inductor core temperature was allowed to stabilise.

Table 7: PFC efficiency for a 230VAC input

Power level (watts)	Efficiency (%)
492	96.7
953	98.3
1587	97.2
2580	95
2970	94

The theoretical calculations placed the worst case efficiency at 90%. The calculations also made assumptions due to the lack of information in the APT5012 datasheet. The results depicted in Table 7 do however compare favourably with those reported in the literature.

9.1.4 Harmonic analysis

In Figure 70, the input current waveform is a clean and distortion-free sine wave in phase with the voltage. However closer analysis of the waveform - in Figure 75 - reveals some cusp distortion.

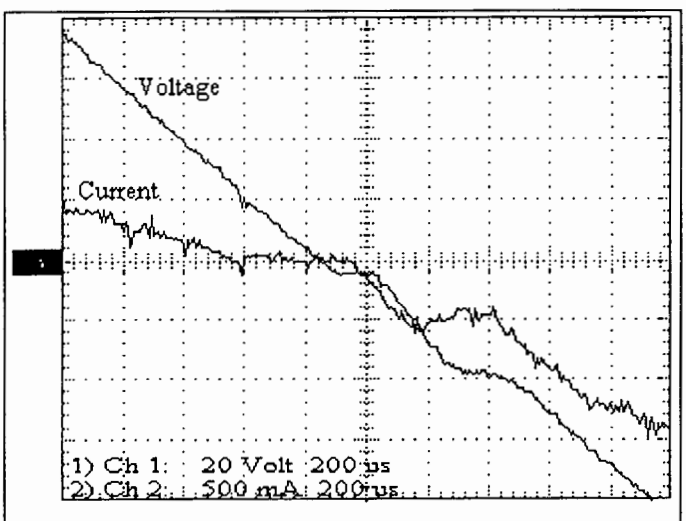

Figure 75: Line current distortion at the voltage zero-crossing

When the input voltage is near zero, the voltage across the inductor is small. This prevents the current from tracking the programmed value. The length of time that the current does not track the reference is a function of the inductor value. The distortion is minimised by reducing the inductor value but at the expense of a higher ripple current.

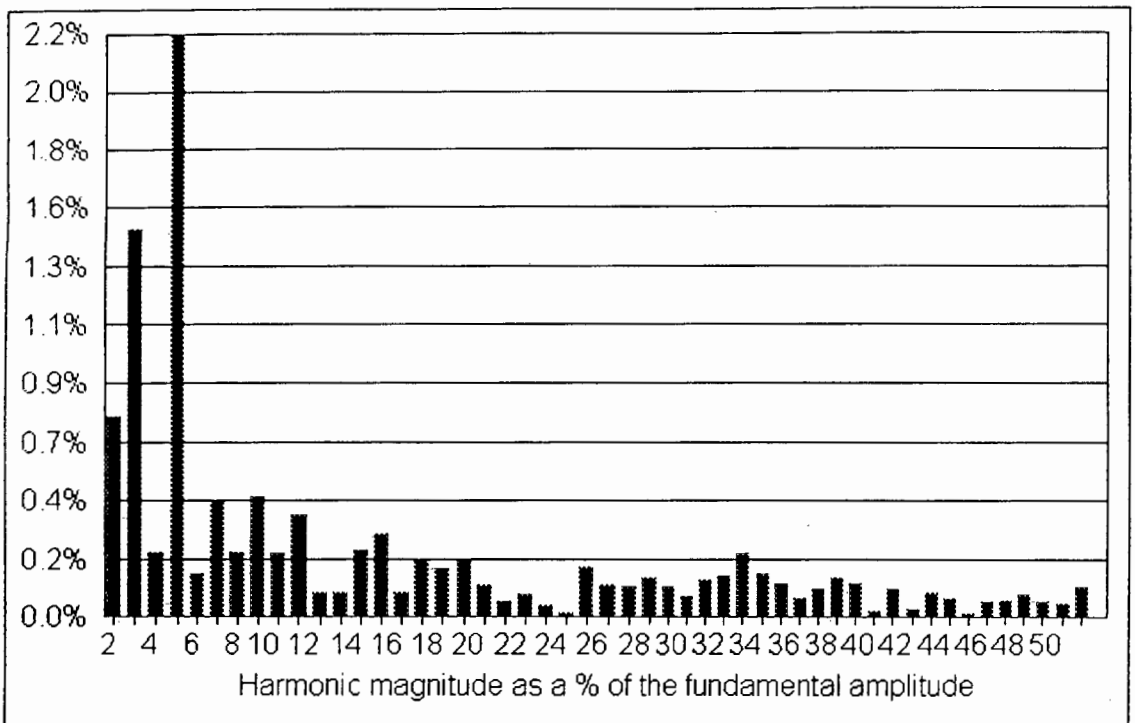

Figure 76: Line voltage harmonics

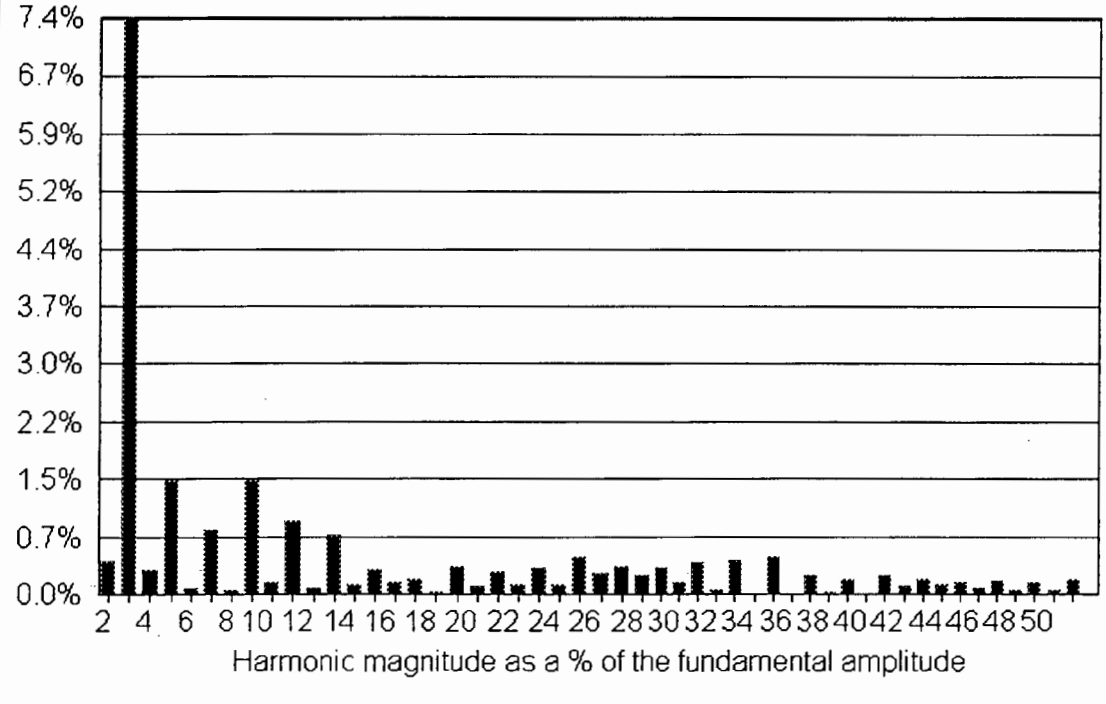

Figure 77: Current harmonics

The voltage harmonics depicted in Figure 76 remained relatively unchanged during testing. The current harmonics in Figure 77 also varied little over the entire load range. Both the power factor at 0.99 and $THD < 4\%$ are within the design specifications.

9.2 IGBT Inverter

9.2.1 Experimental set-up

A three phase variac and rectifier was used to supply the DC bus voltage through a 25 amp circuit breaker. True RMS meters were then used to record current and voltage data while all oscillograms were captured using a HP54601B oscilloscope and uploaded to the PC using ScopeLink V2.02.

The magnitude, frequency and phase of the inverter output was controlled from the PC through an RS232 link. Both the PC and oscilloscope where powered through an isolation transformer.

9.2.2 Commissioning the inverter system

To commission the inverter, the following parameters were downloaded into the controller via the RS232 link:

$$f_s = 6.2kHz \qquad f_m = 50Hz \qquad M_a = 0.9$$

A resistive load equal to 10% ($R_{Load} = 105.8\Omega$) was attached directly to the inverter output. The DC bus voltage was systematically increased to $V_{DC} = 380V$ while continually monitoring the voltage across the IGBTs, the DC bus and load current. As no problems were encountered, the inverter load was increased.

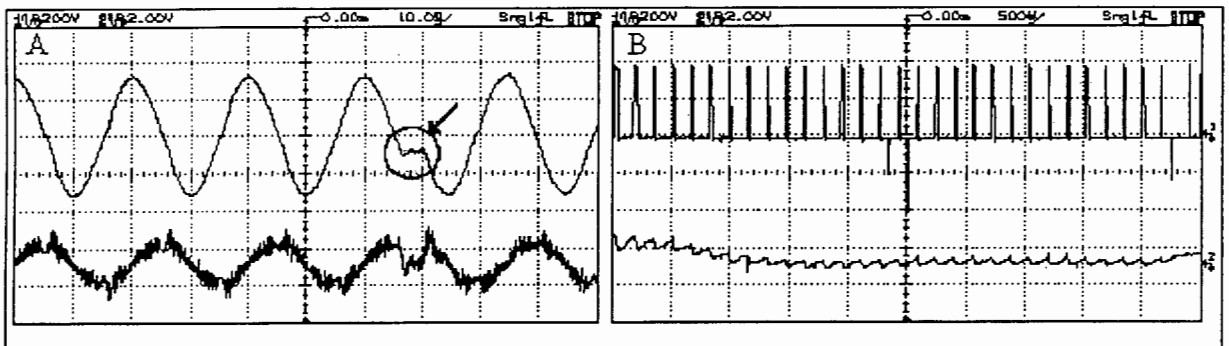

Figure 78: Controller reset as a result of EMI

Once the load current exceeded 14.5 amps, the operation of the controller became impaired by random resetting as illustrated in Figure 78A. The upper trace is the inverter output voltage after the LC-filter. The distorted current through the filter capacitor is shown in the lower trace. In Figure 78B, the reset and its effect on the output voltage is illustrated in greater detail. This behaviour also resulted in noise from

the filter inductor. The problem was solved by shielding the controller with a grounded aluminium plate mounted on top of the PCB. Alternatively the heatsink could form the shield by mounting the controller below the heatsink.

The output of the inverter at maximum load (230Vrms, 22Arms) is given Figure 79A. As evidenced, the DC bus voltage tends to collapse towards the peak of each half cycle. By synchronising the inverter load current with the incoming phase voltage, the DC bus ripple can be minimised. This is illustrated in Figure 79B.

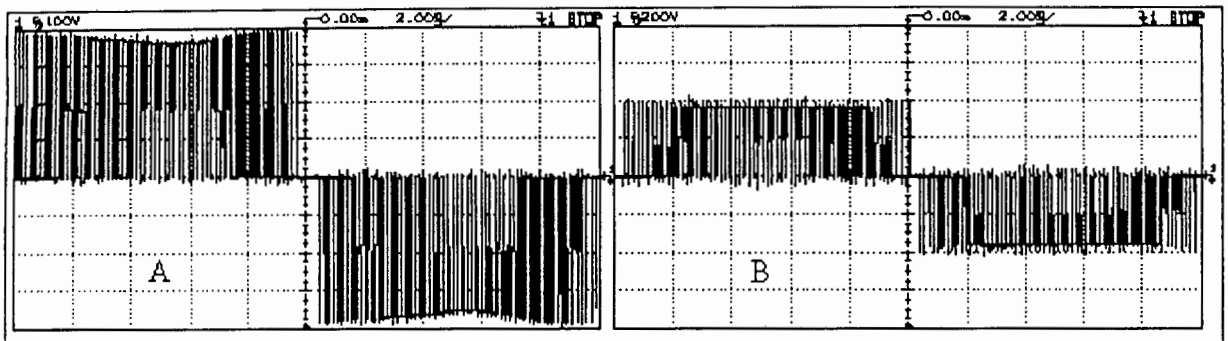

Figure 79: Inverter output under maximum load

While operating at maximum power output, closer examination of the PWM waveform revealed the pulse discrepancy indicated below in Figure 80.

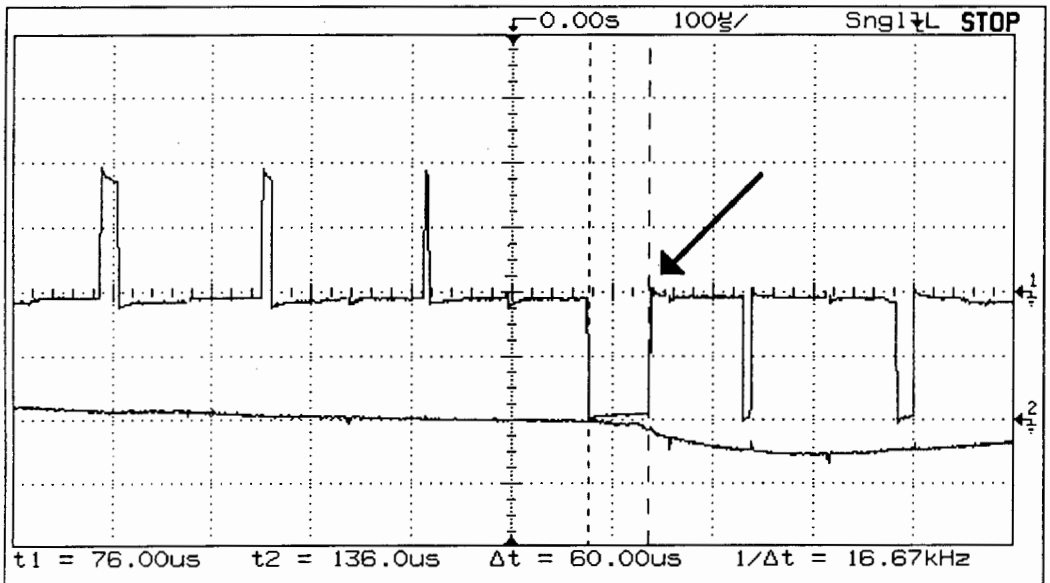

Figure 80: Pulse discrepancy in the PWM stream

With further examination, it was determined that the pulse occurred every fifth output cycle. Because of its regularity, the software was scrutinised and debugged. The failure to clear the carry flag in the output amplitude routine (Ma adjustment) resulted in the erroneous generation 0xE5 every fifth cycle instead of 0x80. The difference of 0x65 was responsible for a 62.88us - 2.7us (SKHI21 dead-time) = 60.18us pulse as illustrated.

With the voltage regulation loop, DC bus ripple regulator, communications interface and system management enabled, the microcontroller stack overflowed erratically. This was caused by the microcontroller being unable to completely process an interrupt routine before the same interrupt occurred once more.

The solution is usually to code interrupt service routines in assembler for speed or re-arrange interrupt priorities. In this case, a profiler[48] revealed the lack of processing power. To store a digitised voltage or current consumed 12us (18 cycles). A single floating-point multiply cost anything up to 153us (230 cycles). Even with the PWM update hand-coded and optimised in assembler, only 43% of the processing time remained.

To alleviate the problem, the PWM update rate was reduced from 6.41kHz to 4.394kHz. This reduced the number of ADC conversions and floating point operations required. The effect of these changes on the transient performance of the inverter are documented in section 9.3.2.

9.2.3 Harmonic analysis

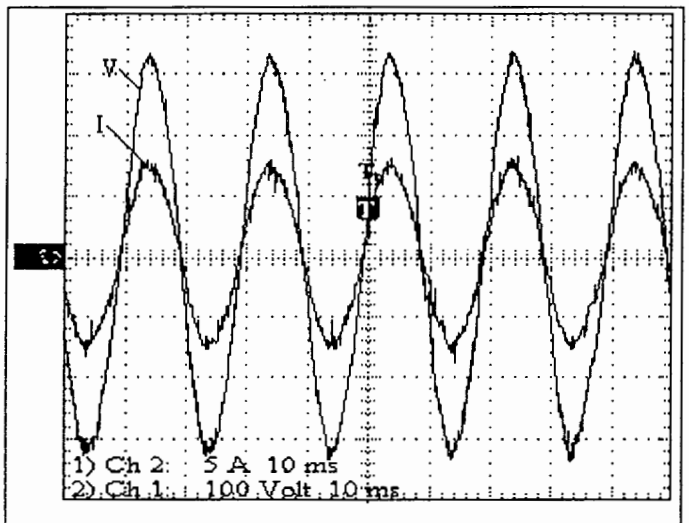

Figure 81: Inverter voltage and current for a 1.2kW resistive load

The voltage and current waveforms of Figure 81 were decomposed using the advanced analysis features built into the THS720P oscilloscope. The harmonics are displayed in Table 8.

[48] A profiler is an analysis tool used to examine the run-time behaviour of a program. Using the profiler information, it can be determined which sections of code are being executed, their sequencing, efficiency and time taken to execute.

Table 8: Inverter output harmonic analysis

	Frequency	Voltage RMS	Voltage % F	Voltage Phase	Current RMS	Current % F	Current Phase
Fundamental	49.9 Hz	228 V	100.00%	0.0	5.21 A	100.00%	0.0
Harmonic 2	99.9 Hz	1.81 V	0.80%	51.8	22.3 mA	0.43%	-29.9
Harmonic 3	150 Hz	4.89 V	2.15%	-88.6	133 mA	2.55%	-87.8
Harmonic 4	200 Hz	668 mV	0.29%	130	16.3 mA	0.31%	137
Harmonic 5	250 Hz	1.19 V	0.52%	-173	26.9 mA	0.52%	-178
Harmonic 6	300 Hz	246 mV	0.11%	-32.4	9.36 mA	0.18%	15.6
Harmonic 7	349 Hz	1.25 V	0.55%	-10.1	23.9 mA	0.46%	-916 m
Harmonic 8	399 Hz	485 mV	0.21%	72.7	11.4 mA	0.22%	78.5
Harmonic 9	449 Hz	2.99 V	1.31%	69.6	71.2 mA	1.37%	64.4
Harmonic 10	499 Hz	348 mV	0.15%	148	16.1 mA	0.31%	111
Harmonic 11	549 Hz	737 mV	0.32%	123	20 mA	0.38%	125
Harmonic 12	599 Hz	185 mV	0.08%	19.7	14.2 mA	0.27%	-130
Harmonic 13	649 Hz	252 mV	0.11%	101	5.59 mA	0.11%	38.8
Harmonic 14	699 Hz	295 mV	0.13%	-142	3.11 mA	0.06%	-110
Harmonic 15	749 Hz	426 mV	0.19%	130	15.5 mA	0.30%	111
Harmonic 16	799 Hz	205 mV	0.09%	138	6.45 mA	0.12%	-92.3
Harmonic 17	849 Hz	132 mV	0.06%	-127	11.2 mA	0.22%	179
Harmonic 18	899 Hz	217 mV	0.10%	95.9	9.9 mA	0.19%	-126
Harmonic 19	949 Hz	207 mV	0.09%	-176	5.96 mA	0.11%	-65.7
Harmonic 20	999 Hz	129 mV	0.06%	-63	7.52 mA	0.14%	-69.6
Harmonic 21	1.05 kHz	102 mV	0.04%	94	5.39 mA	0.10%	17.7
Harmonic 22	1.1 kHz	73.4 mV	0.03%	-59.2	9.85 mA	0.19%	-31.3
Harmonic 23	1.15 kHz	94.7 mV	0.04%	25.1	9.24 mA	0.18%	70.8
Harmonic 24	1.2 kHz	50.7 mV	0.02%	174	10 mA	0.19%	-130
Harmonic 25	1.25 kHz	5.85 mV	0.00%	-154	8.13 mA	0.16%	13.3
Harmonic 26	1.3 kHz	112 mV	0.05%	-23.7	1.83 mA	0.04%	-165
Harmonic 27	1.35 kHz	110 mV	0.05%	14.9	11.4 mA	0.22%	68.8
Harmonic 28	1.4 kHz	109 mV	0.05%	69.2	7.98 mA	0.15%	-175
Harmonic 29	1.45 kHz	53.2 mV	0.02%	118	9.27 mA	0.18%	85.2
Harmonic 30	1.5 kHz	51 mV	0.02%	47	9.76 mA	0.19%	-57.2
Harmonic 31	1.55 kHz	66.4 mV	0.03%	-157	6.18 mA	0.12%	-38.2
Harmonic 32	1.6 kHz	140 mV	0.06%	-151	5.77 mA	0.11%	-133
Harmonic 33	1.65 kHz	56.3 mV	0.02%	-79.3	16.9 mA	0.32%	-104
Harmonic 34	1.7 kHz	87.4 mV	0.04%	-107	5.06 mA	0.10%	69
Harmonic 35	1.75 kHz	114 mV	0.05%	-126	6.12 mA	0.12%	87.2
Harmonic 36	1.8 kHz	114 mV	0.05%	55	4.41 mA	0.08%	-91.1
Harmonic 37	1.85 kHz	246 mV	0.11%	-131	6.26 mA	0.12%	-17.1
Harmonic 38	1.9 kHz	181 mV	0.08%	-46	957 uA	0.02%	-66.1
Harmonic 39	1.95 kHz	85.1 mV	0.04%	-169	4.67 mA	0.09%	-45.2
Harmonic 40	2 kHz	59.5 mV	0.03%	103	7.83 mA	0.15%	-139
Harmonic 41	2.05 kHz	182 mV	0.08%	73.8	10.8 mA	0.21%	-29.2
Harmonic 42	2.1 kHz	112 mV	0.05%	-163	5.25 mA	0.10%	72.9
Harmonic 43	2.15 kHz	236 mV	0.10%	-4.02	8.93 mA	0.17%	68.3
Harmonic 44	2.2 kHz	25.8 mV	0.01%	116	4.15 mA	0.08%	54.8
Harmonic 45	2.25 kHz	130 mV	0.06%	160	940 uA	0.02%	2.6
Harmonic 46	2.3 kHz	106 mV	0.05%	-118	2.95 mA	0.06%	-134
Harmonic 47	2.35 kHz	139 mV	0.06%	102	2.87 mA	0.06%	13.5
Harmonic 48	2.4 kHz	107 mV	0.05%	163	7.91 mA	0.15%	-173
Harmonic 49	2.45 kHz	24.1 mV	0.01%	-153	9.88 mA	0.19%	-6.27

Harmonic 50	2.5 kHz	202 mV	0.09%	-155	6.52 mA	0.13%	-123
Harmonic 51	2.55 kHz	74.8 mV	0.03%	123	2.91 mA	0.06%	161

After filtering, the voltage and current have a THD of 2.83% and 3.23% respectively. The output frequency is not exactly 50.00Hz. This discrepancy may compromise systems which rely on line frequency for their operation e.g. clocks, X10 transmission protocol.

9.3 Overall system performance

The following results were obtained with the PFC connected directly to a single-phase outlet. The IGBT inverter was connected to the PFC output while the output filter was switched between various loads. The battery pack was simulated using a 3-phase bridge rectifier, variac and capacitor bank.

9.3.1 DC bus voltage

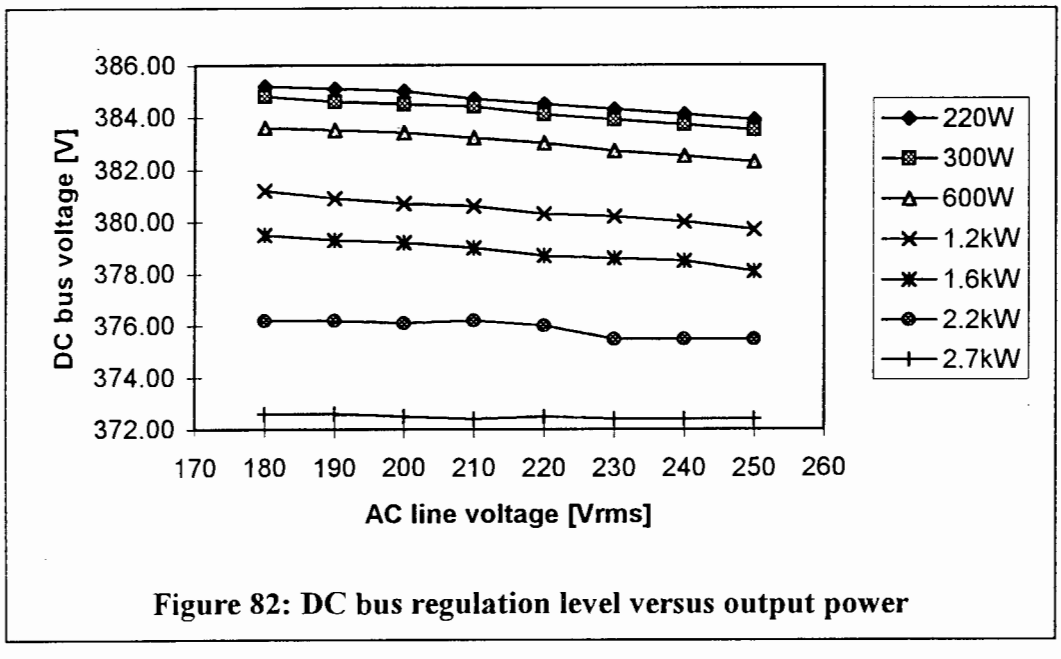

Figure 82: DC bus regulation level versus output power

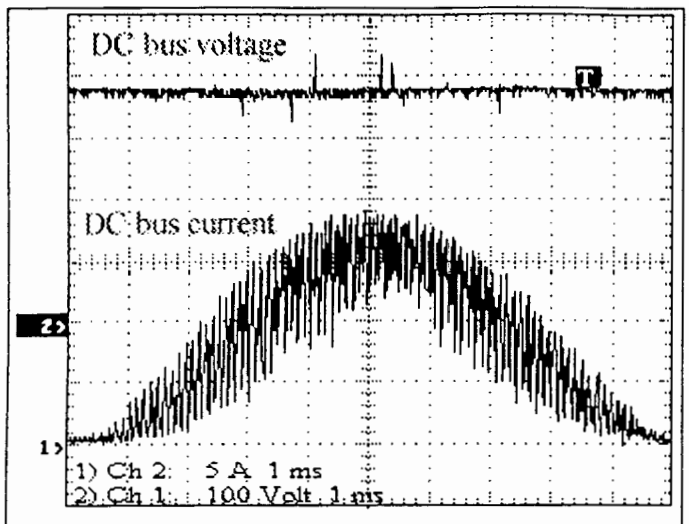

Figure 83: DC bus voltage stability with a 2.7kW load and the ripple regulator enabled

The effectiveness of the PFC voltage regulation loop in reducing the bus impedance is illustrated in Figure 82. At a line voltage of 230Vrms, a load step of 2.5kW results in a 12.8 volt change in the DC bus voltage. The aluminium bus-bar resistance alone is responsible for 4.3V and 60W of losses.

The advantage of synchronising the PFC current and inverter load current is given in Figure 83. The ripple regulator reduced the DC bus voltage ripple under maximum load to approximately 10V. Tighter control should be possible if a 10-bit or 12-bit analogue to digital converter is used on the 400V. In addition, the high frequency ripple could be reduced by synchronising the switching of both the inverter and PFC.

9.3.2 Transient response

The reduction in the PWM update rate described in 9.2.2 moved the zero in the right half s-plane further to the right, comprising both the transient response and stability of the system. The zero is problematic as it introduces a delay into the closed-loop control system. This reduces the phase margin and the allowable loop gain. The lower gain in turn limits the inverters ability to compensate for sudden load changes.

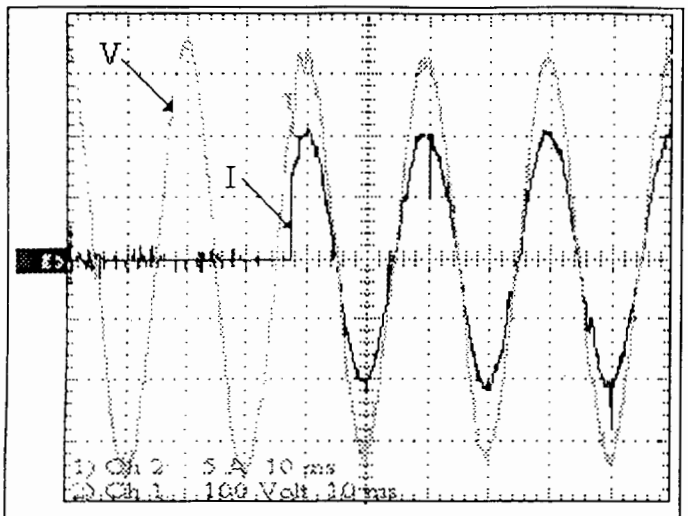

Figure 84: Output voltage collapse on application of a load

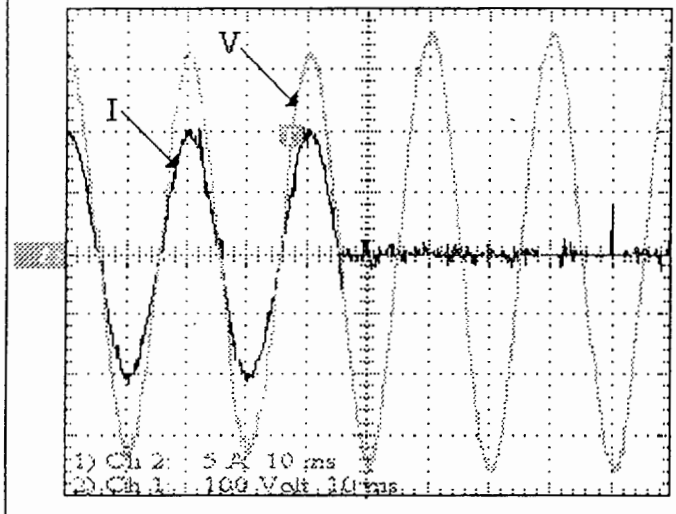

Figure 85: Voltage excursion during the loss of a load

As illustrated in Figure 84, a 1600W load step results in a 7% change in the output voltage - exceeding the design specification of 5%. The output value is also only restored 5 cycles later. A similar situation exists for the loss of the same 1600W load - see Figure 85. The voltage overshoots the set-point by 10% and is restored 5 cycles later. Unlike Figure 84, the output restoration is accompanied by an oscillation whose amplitude increases with the power level.

Voltage feedback alone is not sufficient for AC voltage regulation because of the undamped second-order nature of the LC output filter[49]. An inner current loop, together with an outer voltage control loop, is required to split the undamped LC-filter poles. This will ensure that the closed-loop system is stable and has an acceptable dynamic response. No visible change in the output voltage was observed with a sudden loss of the line voltage and subsequent transfer over to the simulated battery pack.

[49] Jung, S.; Huang H. et al.; "DSP-based multiple-loop control strategy for single phase inverters used in AC power sources", PESC, 1997

9.3.3 Efficiency

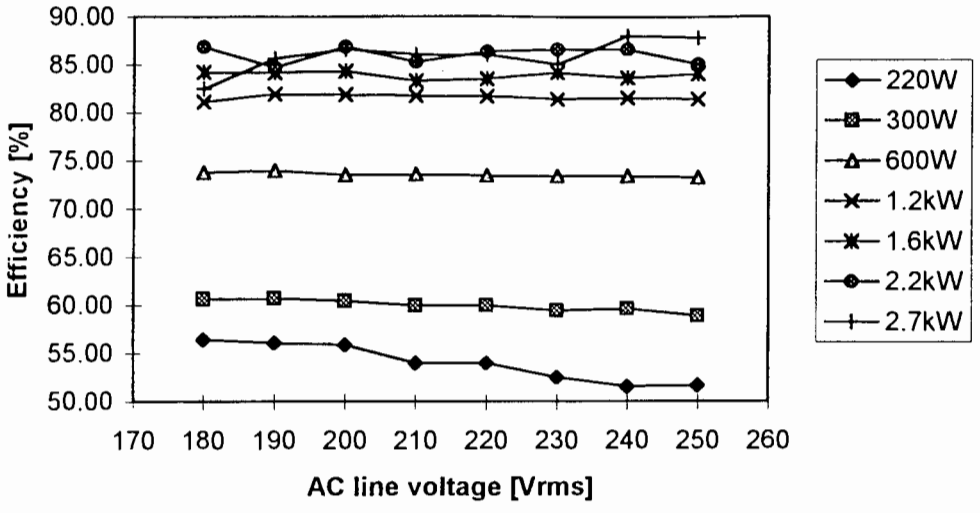

Figure 86: UPS input-output efficiency

The rather low efficiency for a 220 watt load given in Figure 86 is attributable to the 73 watts required by the control electronics ($15V \cdot 863mA = 13W$) and cooling fan (60W). To boost efficiency at low power levels, the PFC and cooling fan should only be enabled when required i.e. during a line swell, a DC bus boost may not be necessary while convection cooling alone may suffice at lower current levels.

Overall, the efficiency of the UPS is 85%, well above the expected 81%. Worst case values were however used throughout the calculations. A large contribution to the this error was the calculated 90% against the measured 94% efficiency for the PFC.

During testing, the boost inductor core temperature was expected to increase by 10°C, whilst in practice it changed very little. This was the result of the extra copper cores added to the Litz wire to reduce both the resistive and frequency dependent loss. The positive temperature coefficient of the MOSFET which would normally have resulted in higher losses at elevated temperatures was curtailed by the reduced heatsink temperature.

The Excel spreadsheet of the experimental results is included in Appendix L.

10. Future Developments

The following are suggestions on how the efficiency, performance or design of the UPS system could be improved.

10.1 Reduction of PFC switching losses

The downside of continuous mode operation is the high turn-on losses of the MOSFET.

During turn-on, the MOSFET diverts the inductor current away from the boost diode. It is during this process that the boost diode exhibits reverse recovery, whereby high levels of reverse current flow until all the stored charge is extracted from its junction region. During this initial phase, the voltage across the diode remains essentially constant, preventing the voltage across the MOSFET from falling. Consequently the MOSFET is forced to conduct the transferred load current and the diode recovery current at a drain-source voltage (V_{ds}) equal to the converter output voltage (≈380V). The losses so created when multiplied by the switching frequency can be horrendous.

Most solutions proposed to reduce the switching losses include an additional semiconductor switch[50]. An alternative is the insertion of a saturable inductance[51] between the boost inductor and MOSFET drain terminal as illustrated in Figure 87.

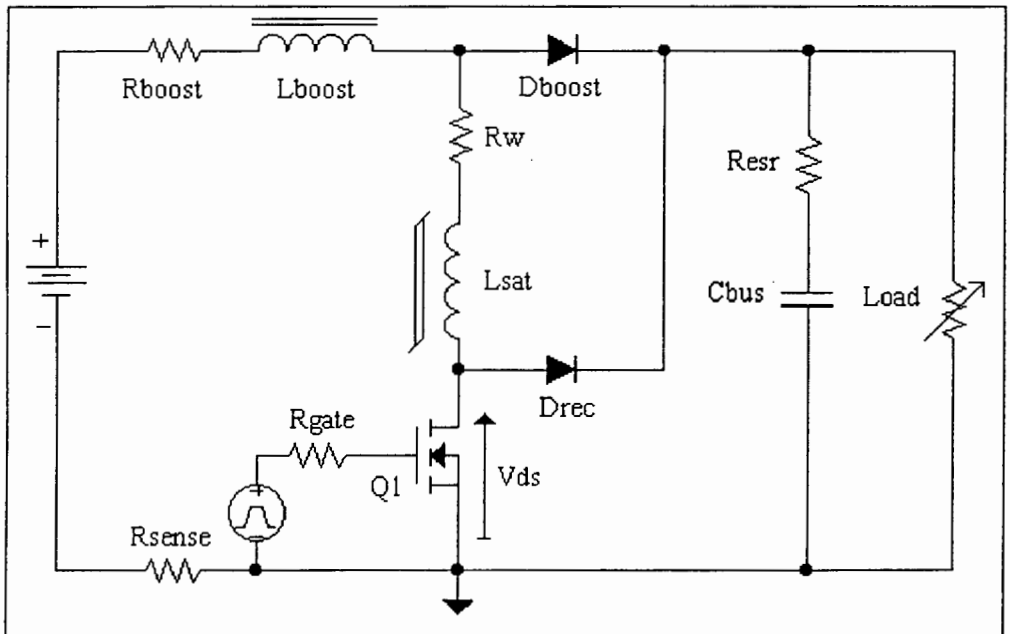

Figure 87: PFC with a loss reducing saturable reactor

[50] Canesin, CA.; Barbi, I.; "A novel single-phase ZCS-PWM high power factor boost rectifier", PESC, 1997

[51] The term "magnetic assist" is also used.

At turn-on, V_{ds} falls towards zero. The only appreciable current flow is the reverse recovery current of D_{rec}[52] and the magnetising current of L_{sat}. After the hold-off time has elapsed, L_{sat} saturates and Q1 conducts both the inductor and boost diode recovery current but at a lower V_{ds}. The net result is a lower turn-on loss and improved system efficiency provided the correct material is chosen for L_{sat}.

To support a large voltage differential for a certain time, L_{sat} must have a high inductive reactance. Once saturated it should present a low inductive reactance. L_{sat} should also switch rapidly between these two states with low loss. These properties can be obtained from a material with an almost square B/H characteristic.

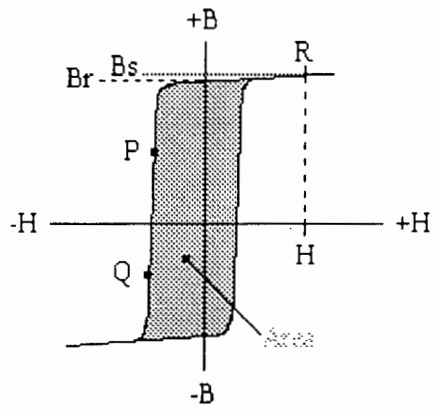

Figure 88: Near-square B/H loop for a saturable inductor

In Figure 88, the slope between the non-saturated points P and Q is almost vertical (very high permeability). This implies a negligible change in H (=NI / ℓ_e) is responsible for the full ΔB excursion. Therefore an inductor wound on this core would have nearly infinite inductance.
In the saturated condition (point R), the characteristic is nearly horizontal. A large change in H generates a negligible change in B. The core permeability is therefore near zero. Once fully saturated, L_{sat} will be equivalent to an air-cored inductor with the same number of turns and dimensions.

The hold-off (volt-seconds) provided by L_{sat} is calculated as follows:

$$V = N \cdot \frac{d\phi}{dt} \qquad \ldots(30)$$

$$\phi = \int B dA \qquad \ldots(31)$$

Substituting (31) into (30) and rearranging yields,

$$V \cdot t = N \cdot \Delta B \cdot A$$

where N = number of turns, ΔB = flux density swing and A = core cross-sectional area.

The power loss in the saturable inductor is a function of the copper and core losses. The copper loss can be controlled by the size, type of wire and the number of turns. The core loss is equal to the area of the hysteresis loop. Core selection should therefore aim for the highest possible unsaturated to saturated permeability ratio. To lower the impedance in the saturated state, the squareness ratio B_r/B_s should be chosen as high as possible. Unfortunately core performance is usually traded-off against cost.

[52] D_{rec} prevents an over-voltage occurring on Q1 during turn-off.

This modification was not tested as access to the MOSFET drain and boost diode anode is not available on the APT5012JNU2 ISOTOP module. The connections are bonded together internally.

10.2 Acoustic noise reduction in the PWM driven IGBT bridge

With the increase in desktop PC's and mainframe computers, many UPS systems are being installed in office environments, generating an awareness amongst manufacturers to the acoustic noise generated by the UPS. This has lead to switching frequencies being placed above or below the audio range.

Industrial applications, particularly the Petrochemical Industry, where UPS's have been connected to induction motor pumps have lead to a different approach. The acoustic noise is generated by the flux within the air-gap of the induction motor at the switching frequency. To avoid the concentration of harmonic energy at distinct tones, the triangular switching frequency is modulated[53] with band-limited white noise[54]. The bandwidth limitation ensures that no low frequency components (and therefore currents) are present at the output. The total acoustic level remains constant, however the acoustic noise generated is more pleasing to the ear due to its random nature.

With a switching frequency well within the audio range, similar approach can be adopted for the current UPS system. The band-limited white noise can be generated off line by a monolithic noise generator, zener diode voltage or a number of other semiconductor methods, digitised and stored within an EPROM. An alternative noise source is a real-time pseudo-noise generator. As the sequence length of the pseudo-noise generator increases, the power spectral density approaches that of white noise[55].

Both aforementioned noise sources have significant disadvantages. The first method requires substantial storage space. The stored sequence should be sufficiently large so as not to effect the PWM output spectra. The second method requires minimal storage but incurs an additional computational burden which increases at approximately $nlog(n^2)$, where n is the register length.

The random number sequence is then used modulate the switching frequency. This can be achieved by periodically reloading the 80C552 microcontroller PWMP register. The effect of the random modulation on the PWM harmonic spectra can be estimated from Carson's Rule,

$$\omega_{BW} = 2 \cdot \omega_n \cdot \left[1 + \frac{\Delta\omega}{\omega_n} \right] \qquad \ldots(32)$$

where ω_n = bandwidth of the injected noise, $\Delta\omega$ = peak frequency deviation.

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[53] Habetler, TG.; Divan, M.; "Acoustic Noise Reduction in Sinusoidal PWM Drives Using a Randomly Modulated Carrier", IEEE Power Elect., Vol. 6, No. 3, July 1991

[54] Constant noise power density per unit bandwidth.

[55] Stremeler, FG.; "Introduction to Communication Systems", 3rd Edition, Addison-Wesley, pp. 439-441, 1990

Assuming a switching frequency of f_s =1kHz, a noise bandwidth of ω_n =500Hz and a peak frequency deviation of $\Delta\omega$=300Hz, Carson's Rule predicts that the energy that was concentrated at f_s will now be spread over a bandwidth of 1600Hz. This is demonstrated graphically in Figure 89.

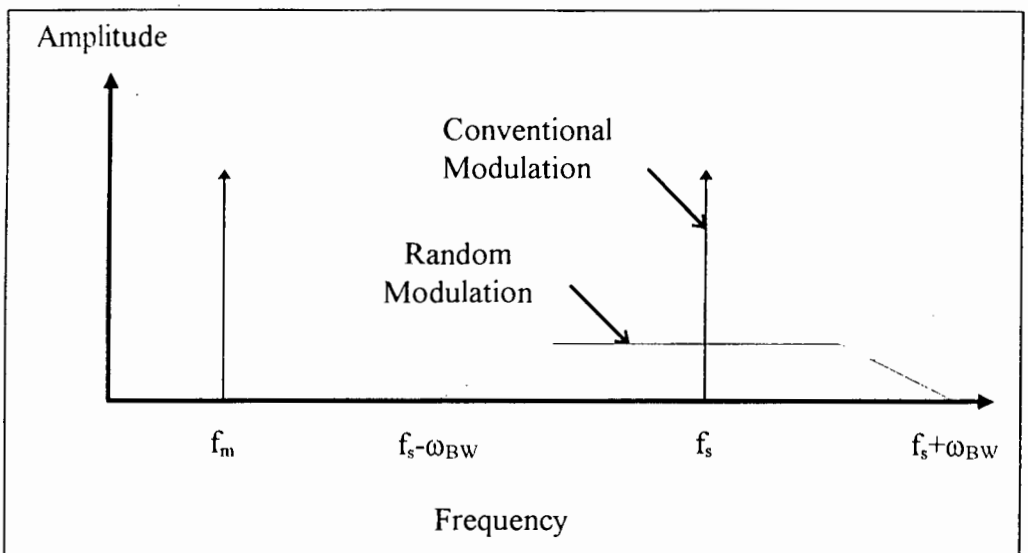

Figure 89: PWM harmonic spectra with a randomly modulated carrier

10.3 A Simplified Topology

The developed topology consists of twelve semiconductor devices. While contributing to the cost of the system, each device also has a negative effect on reliability. By minimising the component count, cost can decreased while the mean time before failure (MTBF) can be increased.

In the topology proposed by Chen et al[56], the load is also supplied via a full bridge inverter. However, the method used to generate the DC bus differs from the developed topology in that a combination of a rectifier and power factor corrector is used. This method reduces the number of semiconductor devices to seven. Refer to Figure 90 .

[56] Chen, C.; Divan, DM.; "Simple Topologies for Single Phase AC Line Conditioning", IEEE TIA, Vol. 30, No. 2, March/April 1994

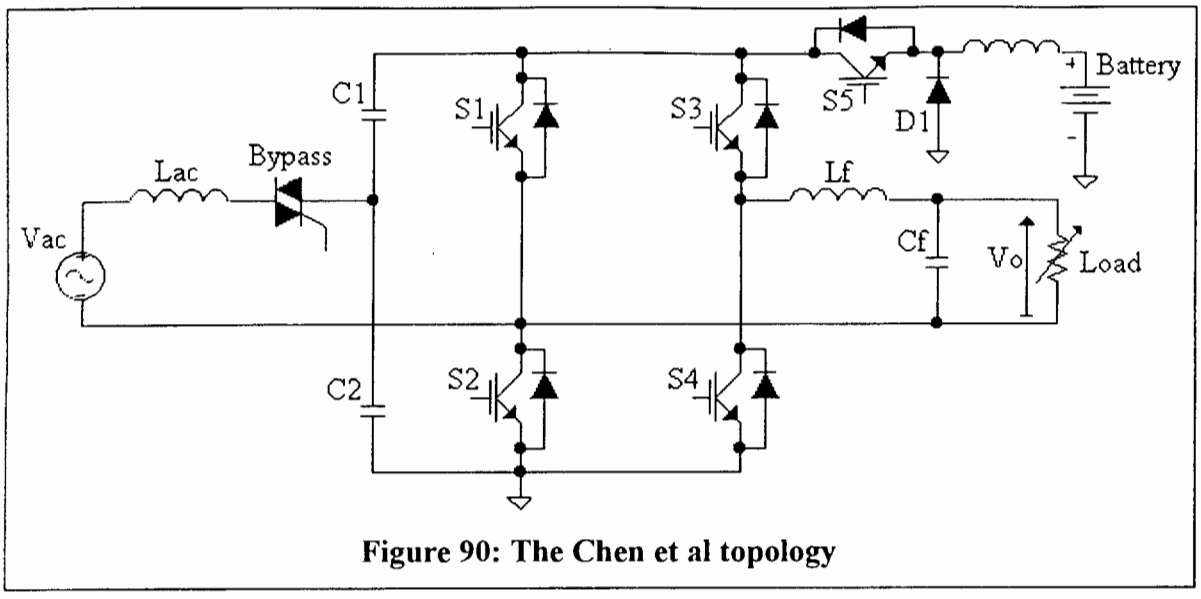

Figure 90: The Chen et al topology

The full bridge inverter consists of the active switches *S1-S4*. The load is connected to the inverter output through the low-pass filter *Lf, Cf*. The reverse recovery diodes in switches *S1, S2* together with *C1, C2* form a voltage doubler. The redundancy provided by the zero states of the full bridge inverter is used to control and shape the input current[57]. Assuming *S1, S2* is driven at a duty cycle d_2 while *S3, S4* at a duty cycle d_1. To satisfy a volt-sec balance implies that,

$$V_{ac} = -d_2 \cdot V_{C1} + (1 - d_2) \cdot V_{C2} \qquad ...(33)$$

While for the output,

$$V_o = V_{ac} - V_{C2} + d_1 \cdot (V_{C1} + V_{C2}) \qquad ...(34)$$

Since d_2 is specified completely by the input voltage and d_1 can vary over the range {0..1}, limits can be obtained for a specified input voltage, controllable voltages V_{C1}, V_{C2} and output voltage. For a sinusoidal trajectory, V_o is bounded by $\{V_{ac}-V_{C2}, V_{ac}+V_{C1}\}$.

During normal operation, the step-down (buck) DC-DC converter formed by *S5, D1* is used to charge the battery pack. When the primary supply fails, the DC bus voltage falls from a maximum of $2V_{ac}$ to V_{bat}, the reverse recovery diode in *S5* is forward biased. The battery pack is then used to maintain the DC bus voltage. The static bypass switch is opened to prevent feedback into the primary supply. With the primary supply disconnected, the inverter switches *S1-S4* are then driven by a standard sinusoidal PWM.

Whether the above system can indeed meet the UPS design criteria (load regulation, harmonic distortion etc.) remains to be investigated.

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[57] Divan, DM.; "Inverter Topologies and Control Techniques for Sinusoidal Output Power Supplies", Conf. Rec., pp. 81-87, APEC' 1991

10.4 Smart battery management

As battery technology continues to evolve, discharge characteristics of the various battery chemistries have become increasingly difficult to predict. What kind of battery chemistry, how many times the battery has been discharged or charged, and self-discharge characteristics are at the root of predicting successfully how long a battery will last under a certain load. Compounding this problem is the fact that without knowledge of the battery's history, it is nearly impossible to calculate predictive data with any accuracy.

The predication accuracy is critical as many sub-systems depend on the UPS. If the UPS is unable to supply the loads for the duration of the power failure, it must be in a position to notify the connected loads well in advance. This will give the various systems a chance to shutdown reliably. If priority scheduling is active, load shedding can extend the expected run-time by retaining only the highest priority load e.g. life-support systems in a hospital.

Clearly, the best solution to this problem is for the battery to keep track of these variables itself. Recognising this as a problem area for most battery powered devices, Duracell and Intel have jointly created a standardised battery system (SBS) interface (Figure 91). A brief description of this host-battery interface specification is now given.

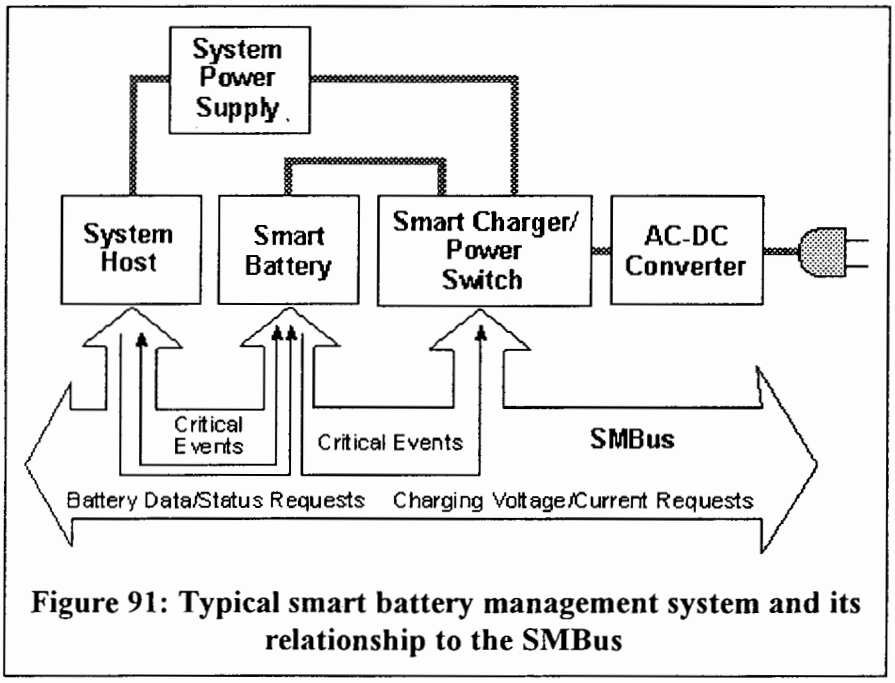

Figure 91: Typical smart battery management system and its relationship to the SMBus

A "smart battery" exhibits an increased level of self-awareness, knowing such things as what its chemical composition is, what the manufactured capacity is, what types of controls are needed when charging and when to terminate operation due to low voltage. By allowing the battery to monitor its own parameters, a host system can request and obtain accurate data allowing it to accurately predict how long the battery

will last under a given load. Using this information, the host can control its operation and/or inform the user how much more operational time they can expect.

The second major component of the SBS specification is the smart battery system bus (SMBus). It is a two-wire bi-directional interface which handles the data communication between the various SBS components. It is very similar in operation to the Philips I^2C interface. Using the SMBus, the host can program the battery to automatically broadcast an alarm message when the remaining capacity is below a certain threshold. This capability removes the need to continuously monitor the battery's condition. In a UPS system this would result in a fractional extension in run-time as less energy is wasted through polling.

The third component is the smart battery charger (SBC). A smart charger allows the battery to control its own charging. A smart battery will tell the charger how to adjust the charging cycle based on its current state of discharge, current temperature, charge / discharge cycle count to date. The charger is also in the position to request the battery chemistry, manufactured capacity and related data and then select an optimal charging algorithm based on this information. A smart battery can also be configured to generate alarm messages to control the battery's charging. By letting the battery automatically issue alarm messages to the charger, the burden of constant monitoring is again eliminated.

The net result of using SBS in a UPS system would be higher reliability and lower maintenance costs as batteries would be reconditioned or replaced less frequently.

A copy of the specification can be found at http://developer.intel.com/ial/powermgm

12. Conclusions

1. A microcontroller-based power supply requires the use of efficient software, the appropriate application of the on-chip A/D converter and PWM circuits, as well as attention to computational delay, word length, calculation precision and sampling frequency.

2. Careful component layout combined with the judicious use of PCB ground planes is not always sufficient. Additional shielding is mandatory where large high frequency currents and voltages are concerned.

3. The processing power required to perform a specific task is often under estimated.

4. It is the lack of processing power, precluding the use of floating point or an optimal control algorithm, which ultimately compromises the performance of the system.

13. Recommendations

1. A 16-bit microcontroller or low-end digital signal processor (DSP) will provide the extra processing power needed to optimise the UPS response.

2. The full-bridge rectifier, in-rush current limit combination of a resistor and bypass relay should be replaced with an integrated thyristor-diode bridge module. The current can then be controlled by adjusting the thyristor firing angle.

3. The boost inductor AC flux density should be increased from around 50gauss to a more cost-effective 400gauss. This is possible with a smaller T400-26D core whilst still maintaining the required output power level.

4. The entire power factor corrector assembly must be enclosed in a metal cabinet to shield both test-equipment and user equipment from EMI.

5. The DC-bus electrolytic capacitors should be replaced with film dielectric capacitors (e.g. ULYTIC™) as they offer a ten-fold increase in current density; three times the over-voltage capability and better temperature stability over the -55°C to 85°C range.

6. The IGBTs should be replaced with the third generation devices as they offer a lower on-state voltage drop and faster switching times. The power MOSFET devices available from Motorola and International Rectifier should be considered at higher switching frequencies.

7. Increasing the inverter switching frequency will allow a smaller output filter. Assuming the control algorithms are adjusted accordingly, this reduction in energy storage will help improve the transient response.

8. The power factor corrector output voltage should be a function of both the incoming line voltage and the inverter set-point to maximise system efficiency.

9. To facilitate converter testing, standard laboratory equipment should include a high power variable load bank with an adjustable power factor.

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Appendix A: Evaluation of the PWM method used to drive the IGBT inverter

The following MathCAD script was used to evaluate the PWM method

Inverter Output frequency: $f_1 := 50$ $\omega := 2 \cdot \pi \cdot f_1$ $\omega = 314.159$

Average DC-bus voltage: $Vb := 380$

Desired RMS output voltage: $Vrms := 230$

Calculate the modulation amplitude: $ma := \frac{230 \cdot \sqrt{2}}{380}$ $ma = 0.856$

The inverter switching frequency has purposely been reduced for clarity when displaying graphics.

Inverter switching frequency: $fs := 500$

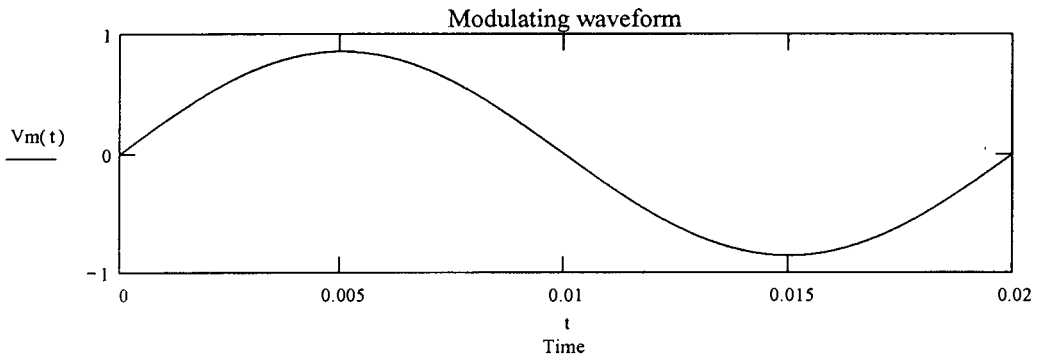
Frequency modulation ratio: $mf := \frac{fs}{f_1}$ $mf = 10$

The 80C552 microcontroller generates "regularly sampled PWM" with the rising edge occuring every 1/fs seconds while the trailing edge is modulated.

The modulating function is given by: $Vm(t) := ma \cdot \sin(\omega \cdot t)$

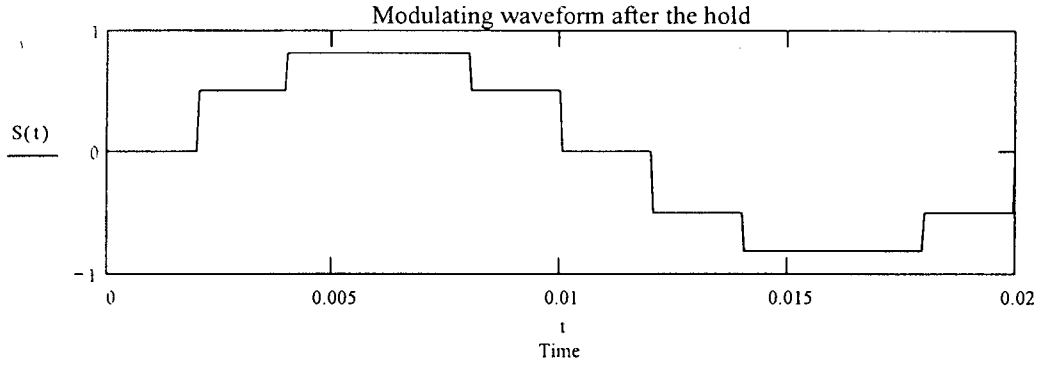
Viewed over a single cycle, the modulating waveform appears as follows:

$t := 0, 0.00005 .. \frac{1}{f_1}$



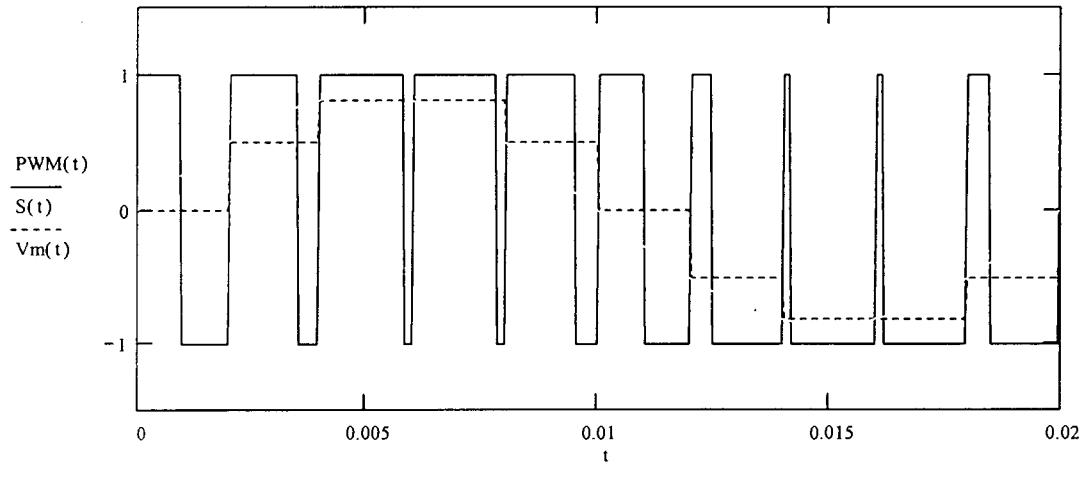
Internally, the microcontroller samples Vm(t) every 1/fs seconds and holds the sampled value until the next sampling instant. This is equivalent to convolving Vm(t) with a train of unit-impulses followed by a zero-order hold.

$$S(t) := Vm\left(t - \mathrm{mod}\left(t, \frac{1}{fs}\right)\right)$$



The sampled value determines the pulsewidth in the current interval. The PWM is then calculated as follows:

$$PWM(t) := \mathrm{if}\left[t > t - \mathrm{mod}\left(t, \frac{1}{fs}\right) + \left(\frac{1 + S(t)}{2 \cdot fs}\right), -1, 1\right]$$



PWM(t) is used to drive the IGBT inverter. The harmonic content of the output is now calculated.

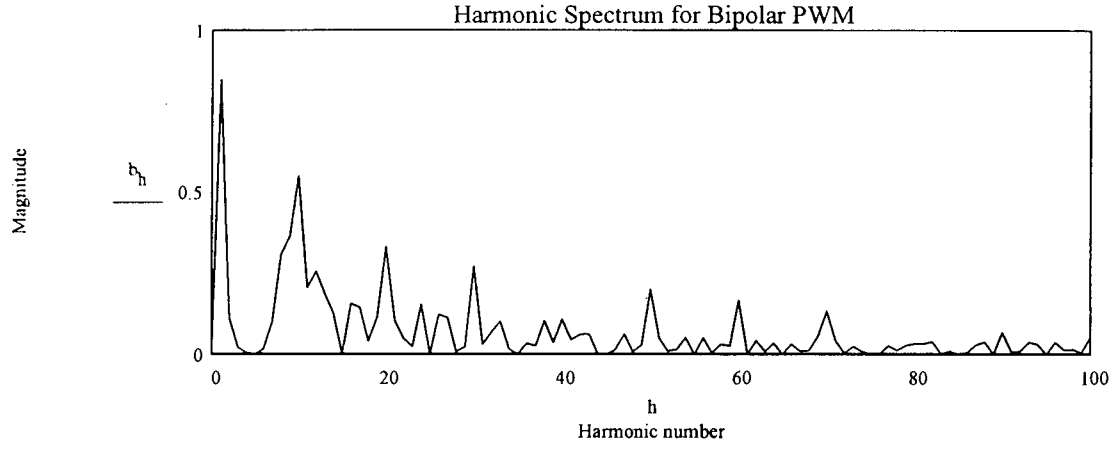
FFT length: $N := 4096$

Sample interval: $\Delta := \frac{\frac{1}{f_1}}{N}$ $\Delta = 4.883 \cdot 10^{-6}$

Form the input vector: $n := 0, 1 .. N - 1$ $u_n := PWM(n \cdot \Delta)$

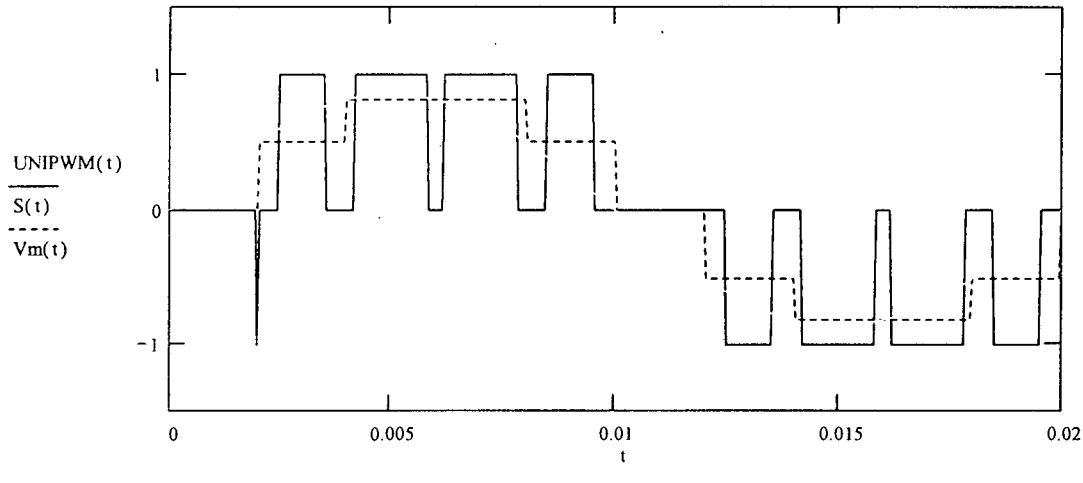
Calculate the Fourier transform: $b := \frac{2}{\sqrt{N}} \cdot \mathrm{fft}(u)$

$h := 0, 1 .. \frac{N}{2}$



The low order harmonics may be pushed higher by driving the inverter with unipolar PWM.

$UNIPWM(t) := \frac{1}{2} \cdot PWM(t) - PWM\left(t + \frac{1}{2 \cdot f_1}\right)$

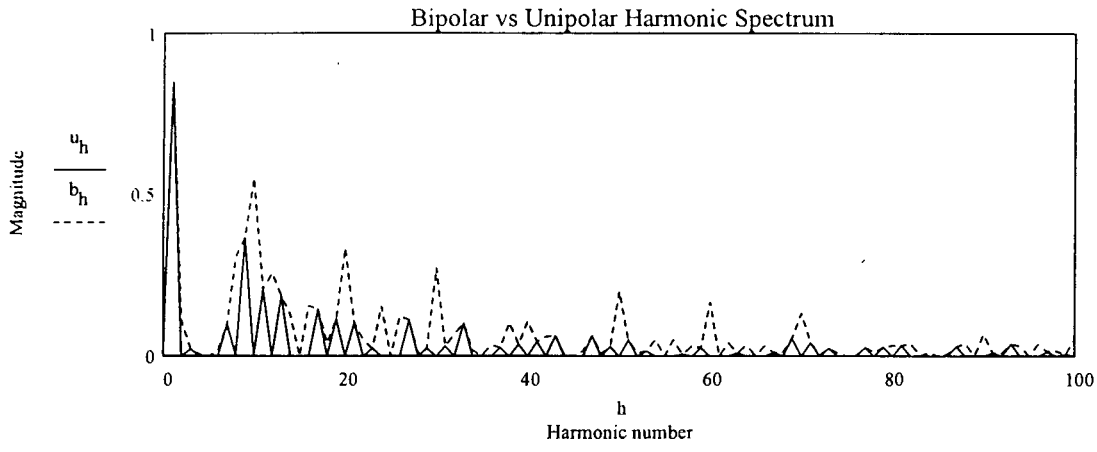


It is interesting to note that unlike conventional unipolar PWM derived from a comparison of a sine and a phase shifted version with a triangular waveform, the microprocessor generated regular sampled PWM does not double the "effective" switching frequency. This is because the only the falling edge is modulated.

Calculating the harmonic spectrum for the unipolar PWM driven bridge yields the following:

Construct vector: $w_n := UNIPWM(\Delta \cdot n)$

Calculate the Fourier transform: $u := \frac{2}{\sqrt{N}} \cdot \mathrm{fft}(w)$



To quantify the reduction in harmonic content, the total harmonic distortion is calculated.

Number of harmonic components to include: $N := 50$

Total harmonic distortion for Bipolar PWM: $bTHD := \frac{\sqrt{\sum_{h=2}^{N} (|b_h|)^2}}{|b_1|}$

$bTHD = 1.247$

Total harmonic distortion for Unipolar PWM: $uTHD := \frac{\sqrt{\sum_{h=2}^{N} (|u_h|)^2}}{|u_1|}$

$uTHD = 0.65$

Difference in totol harmonic distortion for the first N-harmonics: $Diff := bTHD - uTHD$

$Diff = 0.597$

This reduction in the inverter harmonic content reduces the demands on the output filter.

For comparison, the harmonic spectrum and THD is calculated for PWM generated using an analog sinewave - triangular wave comparison.

Define the shape of a triangular wave:

$$\text{Shape}(t) := \begin{cases} t \cdot 4 \cdot fs & \text{if } t \le \frac{1}{4 \cdot fs} \\ 1 - \left(t - \frac{1}{4 \cdot fs}\right) \cdot 4 \cdot fs & \text{if } \frac{1}{4 \cdot fs} < t < \frac{3}{4 \cdot fs} \\ -1 + \left(t - \frac{3}{4 \cdot fs}\right) \cdot 4 \cdot fs & \text{if } t \ge \frac{3}{4 \cdot fs} \end{cases}$$

Force the argument given within 0..1/fs range

$$C(t) := \text{if}\left(\text{mod}\left(t, \frac{1}{fs}\right) = 0, \frac{1}{fs}, \text{mod}\left(t, \frac{1}{fs}\right)\right)$$

Combining gives $\text{Vtri}(t) := \text{Shape}(C(t))$

Next, construct the comparator which will generate a the first part of the PWM waveform

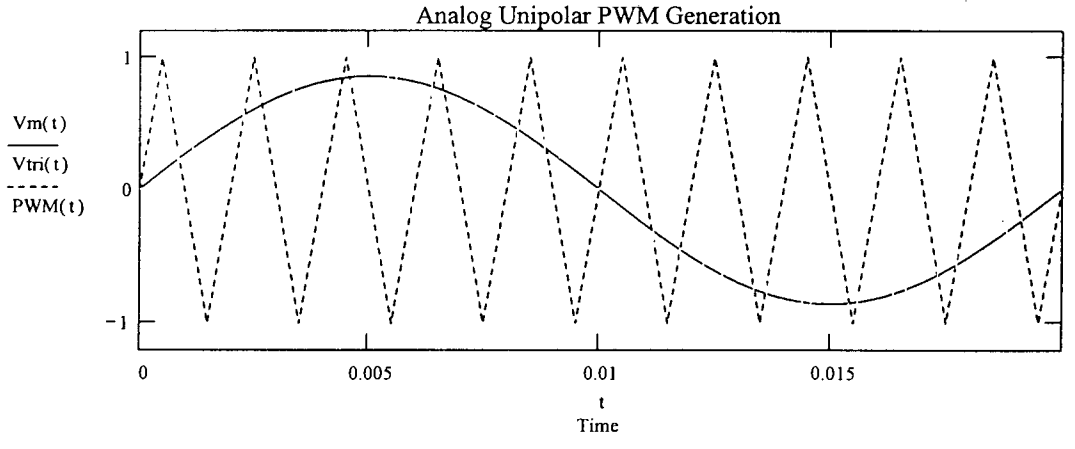
$$\text{LegA}(t) := \text{if}(\text{Vtri}(t) > \text{Vm}(t), 0, 1)$$

Shifting the modulating waveform 180 degrees

$$\text{LegB}(t) := \text{if}\left(\text{Vtri}(t) > \text{Vm}\left(t + \frac{1}{2 \cdot f_1}\right), 0, 1\right)$$

Combine the modulation on both inverter legs to generate the unipolar PWM output

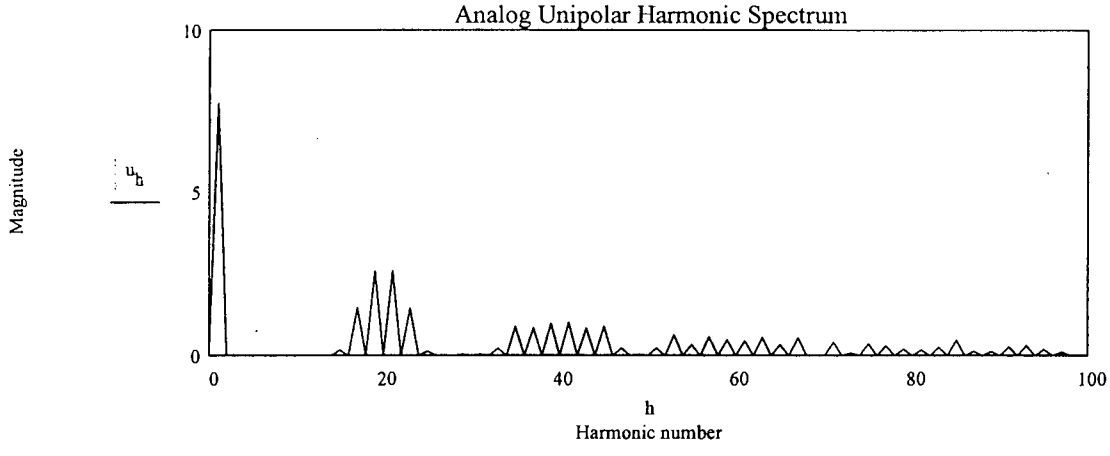
$$\text{PWM}(t) := \text{LegA}(t) - \text{LegB}(t)$$



Calculating the harmonic spectrum for the unipolar PWM driven bridge yields the following:

Construct vector: $w_n := PWM(\Delta \cdot n)$

Calculate the Fourier transform: $u := \frac{2}{\sqrt{N}} \cdot fft(w)$



Calculate the total harmonic distortion for the analog unipolar PWM

$$THD := \frac{\sqrt{\sum_{h=2}^{N} |u_h|^2}}{|u_1|}$$

THD = 0.613

The digitally generated unipolar PWM yielded: uTHD = 0.65

The digital unipolar PWM harmonic distortion is higher than the equivalent analog system because only a single edge is modulated. It can be shown that should both edges be modulated, the digital system will yield an even lower THD than the analog system. The method is however too computationally intensive to be implemented on the current controller hardware.

To implement the analog unipolar PWM system requires more components. As a UPS is meant to have the minimum number of components - the digital unipolar PWM will be implemented. The difference in THD is not excessive. In a redesign of the controller, more processing power will be harnessed (e.g. DSP or 16-bit microcontroller) to generate both rising and falling edge modulated unipolar PWM.

Appendix B: UC3854 Power factor controller design procedure

The following MathCAD script was used to calculate the discrete component values around the UC3854 controller chip

Operating requirements: $Pout := 4375$

$Vout := 380$

$Vmin := 180$ $Vmax := 250$

$fmin := 47$ $fmax := 65$

Select switching frequency: $fs := 100 \cdot 10^3$

Inductor Selection:

Maximum peak line current - $Pin := Pout$

$$Ipk := \frac{\sqrt{2} \cdot Pin}{Vmin} \qquad Ipk = 34.373$$

Ripple current - $Iripple := 0.05 \cdot Ipk$ $Iripple = 1.719$

Determine duty factor - $$D := \frac{Vout - \sqrt{2} \cdot Vmin}{Vout} \qquad D = 0.33$$

Calculate the inductance - $$L := \frac{\sqrt{2} \cdot Vmin \cdot D}{fs \cdot Iripple} \qquad L = 4.889 \cdot 10^{-4}$$

Select Output Capacitor: $V1 := 320$

$Thold := 0.020$

$$Co := \frac{2 \cdot Pout \cdot Thold}{Vout^2 - V1^2} \qquad Co = 4.167 \cdot 10^{-3}$$

$Co := 0.004$

Select the current sensing resistor:

Find maximum current - $$tIpk := Ipk + \frac{Iripple}{2} \qquad tIpk = 35.233$$

Calculate resistor value - $Vrs := 1$

$$Rs := \frac{Vrs}{tIpk} \qquad Rs = 0.028$$

Calculate actual Vrs - $Rs := 0.02$

$Vrs := tIpk \cdot Rs$ $Vrs = 0.705$

Set independent peak current limit:

Select overload current limit - $Iovld := 1.2 \cdot tIpk$ $Iovld = 42.279$

$Vrsovld := Iovld \cdot Rs$ $Vrsovld = 0.846$

$Rpk1 := 10 \cdot 10^3$

$Vref := 7.5$

$Rpk2 := \frac{Vrsovld \cdot Rpk1}{Vref}$ $Rpk2 = 1.127 \cdot 10^3$

Multiplier Setup:

Feedforward voltage divider - $Vav := 0.9 \cdot Vmin$ $Vav = 162$

$Rff1 := 910 \cdot 10^3$ $Rff2 := 91 \cdot 10^3$ $Rff3 := 20 \cdot 10^3$

Given

$$\frac{Vav \cdot Rff3}{Rff1 + Rff2 + Rff3} = 1.414$$

$$\frac{Vav \cdot (Rff2 + Rff3)}{Rff1 + Rff2 + Rff3} = 7.5$$

$$Rff1 + Rff2 + Rff3 = 1 \cdot 10^6$$

$$Find(Rff1, Rff2, Rff3) = \begin{bmatrix} 9.537 \cdot 10^5 \\ 3.757 \cdot 10^4 \\ 8.728 \cdot 10^3 \end{bmatrix}$$

Rvac selection - $Vpk := \sqrt{2} \cdot Vmax$ $Vpk = 353.553$

$Rvac := \frac{Vpk}{250 \cdot 10^{-6}}$ $Rvac = 1.414 \cdot 10^6$

$Rvac := 1.5 \cdot 10^6$

Rset selection - $IACmin := \frac{\sqrt{2} \cdot Vmin}{Rvac}$ $IACmin = 1.697 \cdot 10^{-4}$

$Rset := \frac{3.75}{2 \cdot IACmin}$ $Rset = 1.105 \cdot 10^4$

Rmo selection - $Rmo := \frac{Vrs \cdot 1.12}{2 \cdot IACmin}$ $Rmo = 2.325 \cdot 10^{3}$

Oscillator Frequency:

Calculate Ct - $Ct := \frac{1.25}{Rset \cdot fs}$ $Ct = 1.131 \cdot 10^{-9}$

Current Error Amplifier Compensation:

Amplifier gain at fs - $dVrs := \frac{Vout \cdot Rs}{L \cdot fs}$ $dVrs = 0.155$

$Gca := \frac{5.2}{dVrs}$ $Gca = 33.454$

Feedback resistors - $Rci := Rmo$ $Rci = 2.325 \cdot 10^{3}$

$Rcz := Gca \cdot Rci$ $Rcz = 7.779 \cdot 10^{4}$

Crossover frequency - $fci := \frac{Vout \cdot Rs \cdot Rcz}{5.2 \cdot 2 \cdot \pi \cdot L \cdot Rci}$ $fci = 1.592 \cdot 10^{4}$

Ccz selection - $Ccz := \frac{1}{2 \cdot \pi \cdot fci \cdot Rcz}$ $Ccz = 1.286 \cdot 10^{-10}$

Ccp selection - $Ccp := \frac{1}{2 \cdot \pi \cdot fs \cdot Rcz}$ $Ccp = 2.046 \cdot 10^{-11}$

Harmonic Distortion Budget:

Percentage - $THD := 3$

Voltage Amplifier Compensation:

Output voltage ripple - $Vopk := \frac{Pin}{2 \cdot \pi \cdot 100 \cdot Co \cdot Vout}$ $Vopk = 4.581$

Amplifier output ripple - $Gva := \frac{4 \cdot 0.015}{Vopk}$ $Gva = 0.013$

Feedback network - $Rvi := 510 \cdot 10^{3}$

$Cvf := \frac{1}{2 \cdot \pi \cdot 100 \cdot Rvi \cdot Gva}$ $Cvf = 2.383 \cdot 10^{-7}$

Appendix C: PFC inductor design

The inductor design directly influences the efficiency, maximum output power and overall physical size of the converter.

From Appendix B, the peak inductor energy storage is calculated as:

$$E = \frac{1}{2} \cdot L \cdot i^2 = \frac{1}{2} \cdot 500 \cdot 10^{-6} \cdot 35^2 \cong 0.306J \qquad ...(1)$$

From (1), a T520-28D core was selected using Figure 2. The #26 material is a much lower loss material for operation above 50kHz[1]. Unfortunately the largest core, a T400-26D is only good for a maximum of $0.320J$. This is an insufficient margin as the loss of inductance during startup or an overload condition will result in the destruction of the power MOSFET.

For the T520-28D, $A_L = 90nH / N^2$, therefore:

$$N = \sqrt{\frac{L(nH)}{A_L(nH/N^2)}} = \sqrt{\frac{500000 \cdot 10^{-9}}{90 \cdot 10^{-9}}} \cong 75turns \qquad ...(2)$$

Equation (2) assumes there will be no appreciable drop in inductance with increasing magnetising force (H). However as H increases due to the rectified 50Hz component, the inductance will decrease as the core moves closer to saturation (Figure 1).

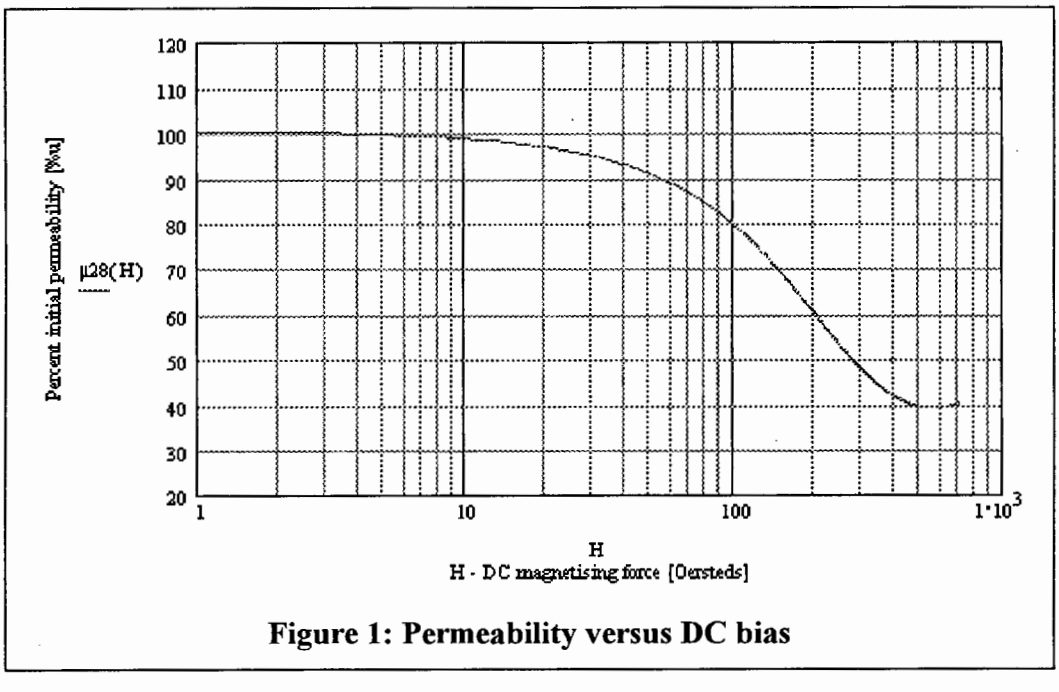


Figure 1: Permeability versus DC bias

[1] 100kHz @ 140gauss: #26=88mW/cm^3; #28=170mW/cm^3

$$\%\mu(H) = \sqrt{\frac{10140 - 30.2 \cdot H + 0.0505 \cdot H^2}{1 + 4.68 \cdot 10^{-4} \cdot H + 1.45 \cdot 10^{-5} \cdot H^2}} \qquad \ldots(3)$$

Combining the percentage drop in permeability (3) with (2), it can be shown that for an inductance of 500uH at 50A (overload), $N = 93$.

The above design is far from optimal as the process was driven by the availability of the various cores from the suppliers.

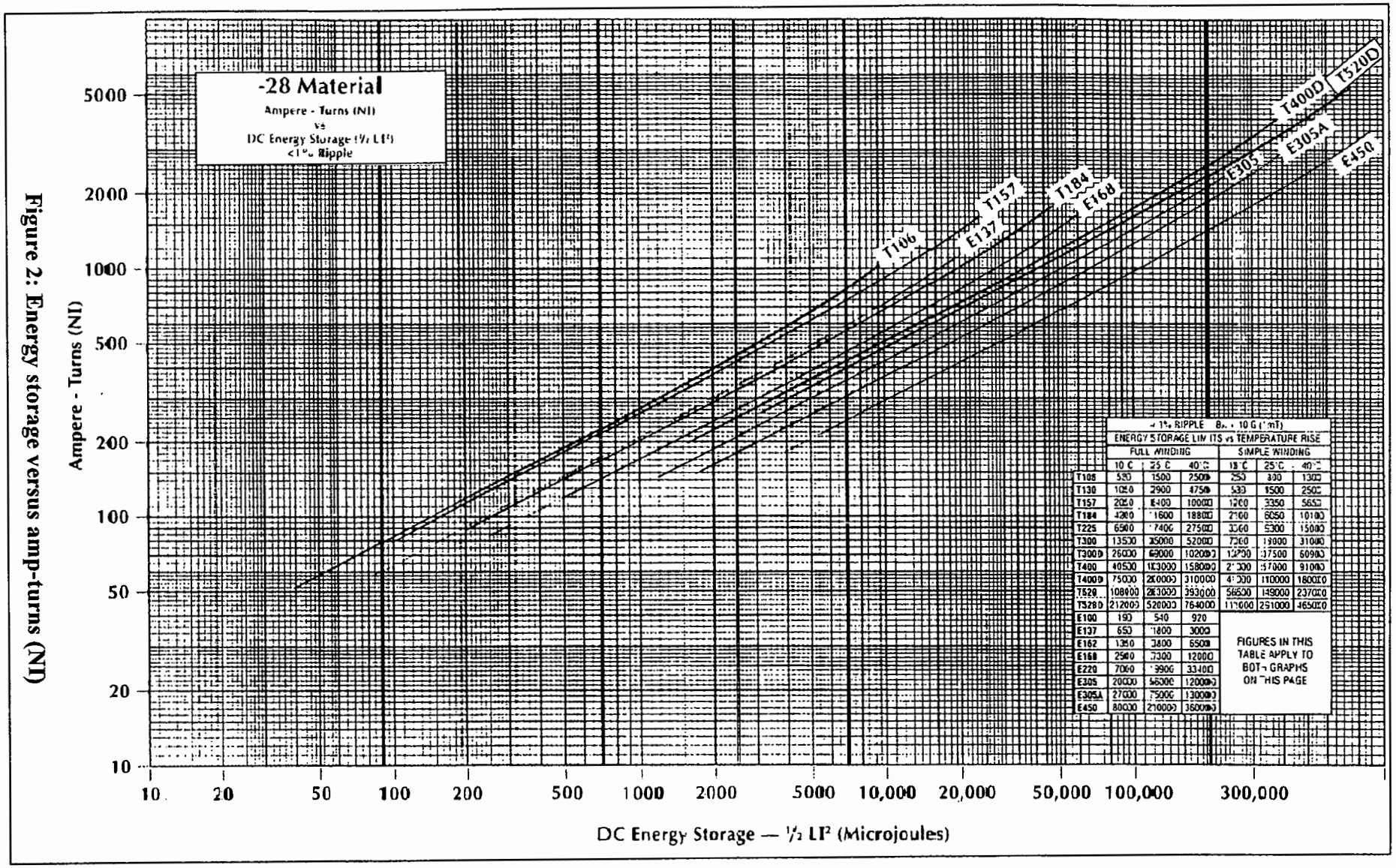


Figure 2: Energy storage versus amp-turns (NI)

Appendix D : Component datasheets

The following datasheets are included:

- 80C552 microcontroller
- APT5012JNU2 power MOSFET
- LT1248 brief
- MC33368D brief
- MG75J2YS50 IGBT
- SKB5012 bridge rectifier
- UC3854 power factor controller

Single-chip 8-bit microcontroller — 80C552/83C552

Single-chip 8-bit microcontroller with 10-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

The 80C552/83C552 (hereafter generically referred to as 8XC552) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552—8k bytes mask programmable ROM
- 80C552—ROMless version of the 83C552
- 87C552—8k bytes EPROM (described in a separate chapter)

The 8XC552 contains a non-volatile 8k × 8 read-only program memory (83C552), a volatile 256 × 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC552 can be expanded using standard TTL compatible memories and logic.

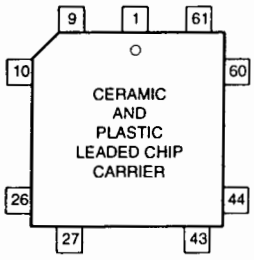
In addition, the 8XC552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16MHz (24MHz) crystal, 58% of the instructions are executed in 0.75µs (0.5µs) and 40% in 1.5µs (1µs). Multiply and divide instructions require 3µs (2µs).

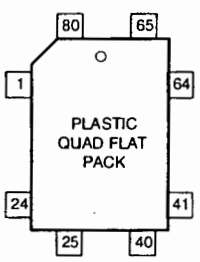
FEATURES

- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 × 8 RAM, expandable externally to 64k bytes
- Capable of producing eight synchronized, timed outputs
- A 10-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three speed ranges:
  - 1.2 to 16MHz
  - 1.2 to 24MHz (ROM, ROMless only)
  - 1.2 to 30MHz (ROM, ROMless only)
- Three operating ambient temperature ranges:
  - PCB83C552–5: 0°C to +70°C
  - PCF83C552–5: –40°C to +85°C (XTAL frequency max. 24 MHz)
  - PCA83C552–5: –40°C to +125°C (XTAL frequency max. 16 MHz)

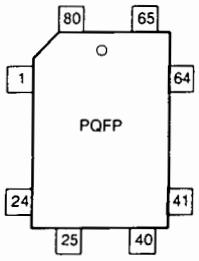
PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWM1}$	39	P2.0/A08
6	$\overline{EW}$	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMSR1	42	P2.3/A11
9	P4.2/CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	46	P2.7/A15
13	P4.6/CMT0	47	$\overline{PSEN}$
14	P4.7/CMT1	48	ALE
15	RST	49	$\overline{EA}$
16	P1.0/CT0I	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6/SCL	56	P0.1/AD1
23	P1.7/SDA	57	P0.0/AD0
24	P3.0/RxD	58	AVref–
25	P3.1/TxD	59	AVref+
26	P3.2/$\overline{INT0}$	60	AV_{SS}
27	P3.3/$\overline{INT1}$	61	AV_{DD}
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/$\overline{WR}$	64	P5.5/ADC5
31	P3.7/$\overline{RD}$	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1



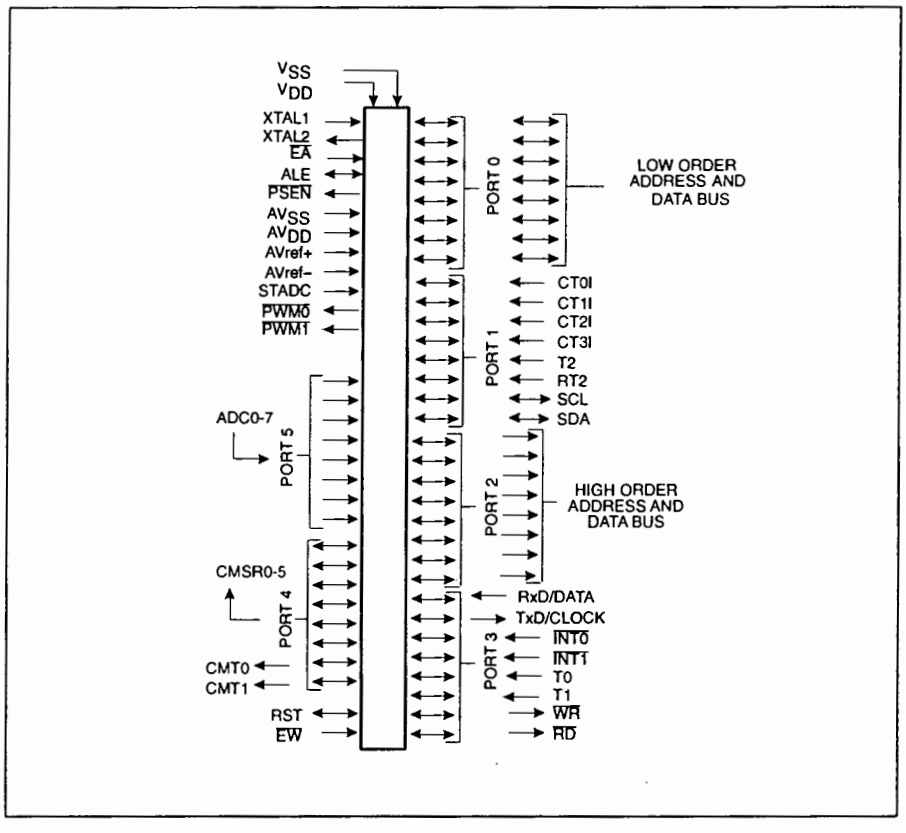
PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P4.1/CMSR1	41	P2.3/A11
2	P4.2/CMSR2	42	P2.4/A12
3	NC	43	NC
4	P4.3/CMSR3	44	NC
5	P4.4/CMSR4	45	P2.5/A13
6	P4.5/CMSR5	46	P2.6/A14
7	P4.6/CMT0	47	P2.7/A15
8	P4.7/CMT1	48	$\overline{PSEN}$
9	RST	49	ALE
10	P1.0/CT0I	50	$\overline{EA}$
11	P1.1/CT1I	51	P0.7/AD7
12	P1.2/CT2I	52	P0.6/AD6
13	P1.3/CT3I	53	P0.5/AD5
14	P1.4/T2	54	P0.4/AD4
15	P1.5/RT2	55	P0.3/AD3
16	P1.6/SCL	56	P0.2/AD2
17	P1.7/SDA	57	P0.1/AD1
18	P3.0/RxD	58	P0.0/AD0
19	P3.1/TxD	59	AVref−
20	P3.2/$\overline{INT0}$	60	AVref+
21	NC	61	AV_{SS}
22	NC	62	NC
23	P3.3/$\overline{INT1}$	63	AV_{DD}
24	P3.4/T0	64	P5.7/ADC7
25	P3.5/T1	65	P5.6/ADC6
26	P3.6/$\overline{WR}$	66	P5.5/ADC5
27	P3.7/$\overline{RD}$	67	P5.4/ADC4
28	NC	68	P5.3/ADC3
29	NC	69	P5.2/ADC2
30	NC	70	P5.1/ADC1
31	XTAL2	71	P5.0/ADC0
32	XTAL1	72	V_{DD}
33	IC	73	IC
34	V_{SS}	74	STADC
35	V_{SS}	75	$\overline{PWM0}$
36	V_{SS}	76	$\overline{PWM1}$
37	NC	77	$\overline{EW}$
38	P2.0/A08	78	NC
39	P2.1/A09	79	NC
40	P2.2/A10	80	P4.0/CMSR0

NC = not connected
IC = internally connected (do not use)

LOGIC SYMBOL



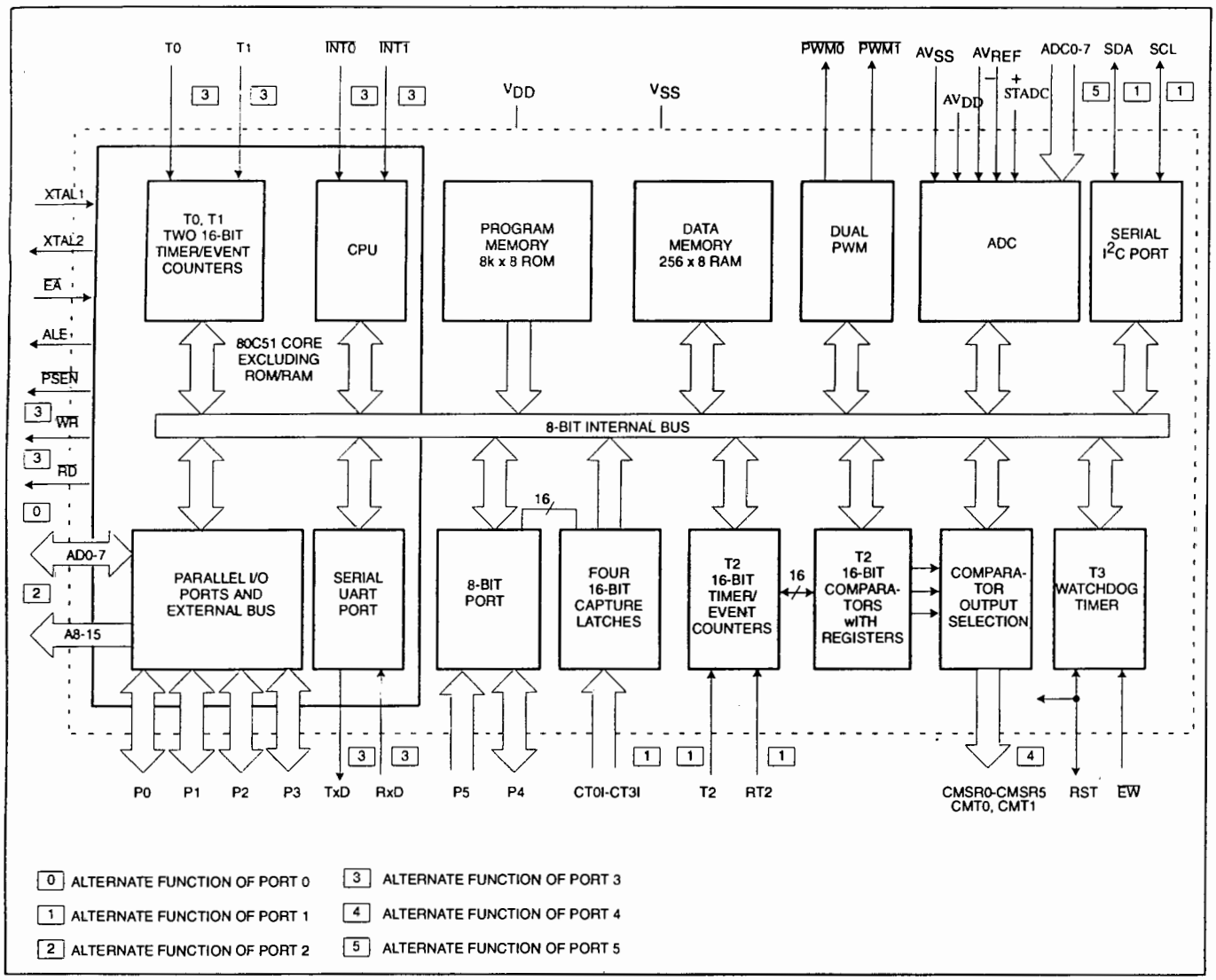
ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		NORTH AMERICA PHILIPS PART ORDER NUMBER		DRAWING	TEMPERATURE °C	FREQ
ROMless	ROM	ROMless	ROM	NUMBER	AND PACKAGE	MHz
PCB80C552-5-16WP	PCB83C552-5WP/xxx	S80C552-4A68	S83C552-4A68	SOT188	0 to +70, Plastic Leaded Chip Carrier	16
PCB80C552-5-16H	PCB83C552-5H/xxx	S80C552-4B	S83C552-4B	SOT318	0 to +70, Plastic Quad Flat Pack	16
PCF80C552-5-16WP	PCF83C552-5WP/xxx	S80C552-5A68	S83C552-5A68	SOT188	–40 to +85, Plastic Leaded Chip Carrier	16
PCF80C552-5-16H	PCF83C552-5H/xxx	S80C552-5B	S83C552-5B	SOT318	–40 to +85, Plastic Quad Flat Pack	16
PCA80C552-5-16WP	PCA83C552-5WP/xxx	S80C552-6A68	S83C552-6A68	SOT188	–40 to +125, Plastic Leaded Chip Carrier	16
PCA80C552-5-16H	PCA83C552-5H/xxx	S80C552-6B	S83C552-6B	SOT318	–40 to +125, Plastic Quad Flat Pack	16
PCB80C552-5-24WP	PCB83C552-5WP/xxx	S80C552-AA68	S83C552-AA68	SOT188	0 to +70, Plastic Leaded Chip Carrier	24
PCB80C552-5-24H	PCB83C552-5H/xxx	S80C552-AB	S83C552-AB	SOT318	0 to +70, Plastic Quad Flat Pack	24
PCF80C552-5-24WP	PCF83C552-5WP/xxx	S80C552-BA68	S83C552-BA68	SOT188	–40 to +85, Plastic Leaded Chip Carrier	24
PCF80C552-5-24H	PCF83C552-5H/xxx	S80C552-BB	S83C552-BB	SOT318	–40 to +85, Plastic Quad Flat Pack	24
PCB80C552-5-30WP	PCB83C552-5WP/xxx	S80C552-CA68	S83C552-CA68	SOT188	0 to +70, Plastic Leaded Chip Carrier	30
PCB80C552-5-30H	PCB83C552-5H/xxx	S80C552-CB	S83C552-CB	SOT318	0 to +70, Plastic Quad Flat Pack	30

NOTE:
1. xxx denotes the ROM code number.

EPROM	DRAWING NUMBER	TEMPERATURE °C AND PACKAGE	FREQ MHz
S87C552-4A68	0398E	0 to +70, Plastic Leaded Chip Carrier	16
S87C552-4K68	1473A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
S87C552-4B	SOT318	0 to +70, Plastic Quad Flat Pack	16
S87C552-5A68	0398E	–40 to +85, Plastic Leaded Chip Carrier	16
S87C552-5K68	1473A	–40 to +85, Ceramic Leaded Chip Carrier w/Window	16
S87C552-5B	SOT318	–40 to +85, Plastic Quad Flat Pack	16

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO. PLCC	PIN NO. QFP	TYPE	NAME AND FUNCTION
V_{DD}	2	72	I	**Digital Power Supply:** +5V power supply pin during normal operation, idle and power-down mode.
STADC	3	74	I	**Start ADC Operation:** Input starting analog to digital conversion (ADC operation can also be started by software). This pin must not float.
$\overline{PWM0}$	4	75	O	**Pulse Width Modulation:** Output 0.
$\overline{PWM1}$	5	76	O	**Pulse Width Modulation:** Output 1.
$\overline{EW}$	6	77	I	**Enable Watchdog Timer:** Enable for T3 watchdog timer and disable power-down mode. This pin must not float.
P0.0-P0.7	57-50	58-51	I/O	**Port 0:** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s.
P1.0-P1.7	16-23	10-17	I/O	**Port 1:** 8-bit I/O port. Alternate functions include:
	16-21	10-15	I/O	**(P1.0-P1.5):** Quasi-bidirectional port pins.
	22-23	16-17	I/O	**(P1.6, P1.7):** Open drain port pins.
	16-19	10-13	I	**CT0I-CT3I (P1.0-P1.3):** Capture timer input signals for timer T2.
	20	14	I	**T2 (P1.4):** T2 event input.
	21	15	I	**RT2 (P1.5):** T2 timer reset signal. Rising edge triggered.
	22	16	I/O	**SCL (P1.6):** Serial port clock line I^2C-bus.
	23	17	I/O	**SDA (P1.7):** Serial port data line I^2C-bus.
				Port 1 is also used to input the lower order address byte during EPROM programming and verification. A0 is on P1.0, etc.
P2.0-P2.7	39-46	38-42, 45-47	I/O	**Port 2:** 8-bit quasi-bidirectional I/O port. Alternate function: High-order address byte for external memory (A08-A15).
P3.0-P3.7	24-31	18-20, 23-27	I/O	**Port 3:** 8-bit quasi-bidirectional I/O port. Alternate functions include:
	24	18		**RxD(P3.0):** Serial input port.
	25	19		**TxD (P3.1):** Serial output port.
	26	20		**$\overline{INT0}$ (P3.2):** External interrupt.
	27	23		**$\overline{INT1}$ (P3.3):** External interrupt.
	28	24		**T0 (P3.4):** Timer 0 external input.
	29	25		**T1 (P3.5):** Timer 1 external input.
	30	26		**$\overline{WR}$ (P3.6):** External data memory write strobe.
	31	27		**$\overline{RD}$ (P3.7):** External data memory read strobe.
P4.0-P4.7	7-14	80, 1-2 4-8	I/O	**Port 4:** 8-bit quasi-bidirectional I/O port. Alternate functions include:
	7-12	80, 1-2 4-6	O	**CMSR0-CMSR5 (P4.0-P4.5):** Timer T2 compare and set/reset outputs on a match with timer T2.
	13, 14	7, 8	O	**CMT0, CMT1 (P4.6, P4.7):** Timer T2 compare and toggle outputs on a match with timer T2.
P5.0-P5.7	68-62, 1	71-64,	I	**Port 5:** 8-bit input port. **ADC0-ADC7 (P5.0-P5.7):** Alternate function: Eight input channels to ADC.
RST	15	9	I/O	**Reset:** Input to reset the 8XC552. It also provides a reset pulse as output when timer T3 overflows.
XTAL1	35	32	I	**Crystal Input 1:** Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock signal when an external oscillator is used.
XTAL2	34	31	O	**Crystal Input 2:** Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external clock is used.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO. PLCC	PIN NO. QFP	TYPE	NAME AND FUNCTION
V_{SS}	36, 37	34-36	I	**Two Digital ground pins.**
$\overline{PSEN}$	47	48	O	**Program Store Enable:** Active-low read strobe to external program memory.
ALE	48	49	O	**Address Latch Enable:** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access, one ALE pulse is skipped. ALE can drive up to eight LS TTL inputs and handles CMOS inputs without an external pull-up.
$\overline{EA}$	49	50	I	**External Access:** When $\overline{EA}$ is held at TTL level high, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at TTL low level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float.
AV_{REF-}	58	59	I	**Analog to Digital Conversion Reference Resistor:** Low-end.
AV_{REF+}	59	60	I	**Analog to Digital Conversion Reference Resistor:** High-end.
AV_{SS}	60	61	I	**Analog Ground**
AV_{DD}	61	63	I	**Analog Power Supply**

NOTE:
1. To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0.5V or V_{SS} – 0.5V, respectively.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol, page 2.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{DD} and RST must come up at the same time for a proper start-up.

IDLE MODE

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

Table 1. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4	PWM0/ PWM1
Idle	Internal	1	1	Data	Data	Data	Data	Data	1
Idle	External	1	1	Float	Data	Address	Data	Data	1
Power-down	Internal	0	0	Data	Data	Data	Data	Data	1
Power-down	External	0	0	Float	Data	Data	Data	Data	1

Serial Control Register (S1CON) – See Table 2

S1CON (D8H)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

Table 2. Serial Clock Rates

CR2	CR1	CR0	BIT FREQUENCY (kHz) AT f_{OSC}					f_{OSC} DIVIDED BY
			6MHz	12MHz	16MHz	24MHz[2]	30MHz[2]	
0	0	0	23	47	62.5	94	117 [1]	256
0	0	1	27	54	71	107 [1]	134 [1]	224
0	1	0	31	63	83.3	125 [1]	156 [1]	192
0	1	1	37	75	100	150 [1]	188 [1]	160
1	0	0	6.25	12.5	17	25	31	960
1	0	1	50	100	133 [1]	200 [1]	250 [1]	120
1	1	0	100	200	267 [1]	400 [1]	500 [1]	60
1	1	1	0.24 < 62.5	0.49 < 62.5	0.65 < 55.6	0.98 < 50.0	1.22 < 52.1	96 × (256 – (reload value Timer 1))
			0 < 255	0 < 254	0 < 253	0 <251	0 < 250	reload value Timer 1 in Mode 2.

NOTES:
1. These frequencies exceed the upper limit of 100kHz of the I²C-bus specification and cannot be used in an I²C-bus application.
2. At f_{OSC} = 24MHz/ 30MHz the maximum I²C bus rate of 100kHz cannot be realized due to the fixed divider rates.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

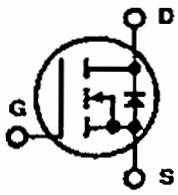
PARAMETER	RATING	UNIT
Storage temperature range	–65 to +150	°C
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Input, output DC current on any single I/O pin	5.0	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.0	W

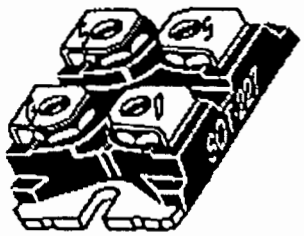
NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DEVICE SPECIFICATIONS

TYPE	SUPPLY VOLTAGE (V)		FREQUENCY (MHz)		TEMPERATURE RANGE (°C)
	MIN	MAX	MIN	MAX	
PCB83(0)C552-5-16	4.0	6.0	1.2	16	0 to +70
PCF83(0)C552-5-16	4.0	6.0	1.2	16	–40 to +85
PCA83(0)C552-5-16	4.5	5.5	1.2	16	–40 to +125
PCB83(0)C552-5-24	4.5	5.5	1.2	24	0 to +70
PCF83(0)C552-5-24	4.5	5.5	1.2	24	–40 to +85
PCB83(0)C552-5-30	4.5	5.5	1.2	30	0 to +70

JHB MASTER





ADVANCED POWER TECHNOLOGY®

APT5010JN 500V 48.0A 0.10Ω
APT5012JN 500V 43.0A 0.12Ω

POWER MOS IV™

SINGLE DIE ISOLATED PACKAGE

N-CHANNEL ENHANCEMENT MODE HIGH VOLTAGE POWER MOSFETS

MAXIMUM RATINGS

All Ratings: T_C = 25°C unless otherwise specified.

Symbol	Parameter	APT 5010JN	APT 5012JN	UNIT
V_{DSS}	Drain-Source Voltage	500	500	Volts
I_D	Continuous Drain Current @ T_C = 25°C	48	43	Amps
I_{DM} I_{LM}	Pulsed Drain Current ① and Inductive Current Clamped	192	172	
V_{GS}	Gate-Source Voltage	±30		Volts
P_D	Total Power Dissipation @ T_C = 25°C	520		Watts
	Linear Derating Factor	4.16		W/°C
T_J,T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150		°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300		

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions / Part Number		MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage (V_{GS} = 0V, I_D = 250 µA)	APT5010JN	500			Volts
		APT5012JN	500			
$I_{D(ON)}$	On State Drain Current ② (V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)}$ Max, V_{GS} = 10V)	APT5010JN	48			Amps
		APT5012JN	43			
$R_{DS(ON)}$	Drain-Source On-State Resistance ② (V_{GS} = 10V, 0.5 $I_{D(Cont.)}$)	APT5010JN			0.10	Ohms
		APT5012JN			0.12	
I_{DSS}	Zero Gate Voltage Drain Current (V_{DS} = V_{DSS}, V_{GS} = 0V)				250	µA
	Zero Gate Voltage Drain Current (V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125°C)				1000	
I_{GSS}	Gate-Source Leakage Current (V_{GS} = ±30V, V_{DS} = 0V)				±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 2.5mA)		2		4	Volts

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.24	°C/W
$R_{\theta CS}$	Case to Sink (Use High Efficiency Thermal Joint Compound and Planar Heat Sink Surface.)			0.05	

⚠ CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

405 S.W. COLUMBIA STREET
BEND, OREGON 97702-1035
U.S.A.

PHONE . . . (503) 382-8028
FAX . . . . . (503) 388-0364

DYNAMIC CHARACTERISTICS

APT5010/5012JN

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	V_{GS} = 0V		5570	6500	pF
C_{oss}	Output Capacitance	V_{DS} = 25V		1170	1640	
C_{rss}	Reverse Transfer Capacitance	f = 1 MHz		440	660	
Q_g	Total Gate Charge ③	V_{GS} = 10V		240	370	nC
Q_{gs}	Gate-Source Charge	V_{DD} = 0.5 V_{DSS}		32	48	
Q_{gd}	Gate-Drain ("Miller") Charge	I_D = I_D [Cont.] @ 25°C		116	170	
$t_{d(on)}$	Turn-on Delay Time	V_{GS} = 15V		15	30	ns
t_r	Rise Time	V_{DD} = 0.5 V_{DSS}		25	50	
$t_{d(off)}$	Turn-off Delay Time	I_D = I_D [Cont.] @ 25°C		48	75	
t_f	Fall Time	R_G = 0.6Ω		12	25	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions		MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)	APT5010JN			48	Amps
		APT5012JN			43	
I_{SM}	Pulsed Source Current ① (Body Diode)	APT5010JN			192	
		APT5012JN			172	
V_{SD}	Diode Forward Voltage ② (V_{GS} = 0V, I_S = -I_D [Cont.])				1.8	Volts
t_{rr}	Reverse Recovery Time (I_S = -I_D [Cont.], dI_S/dt = 100A/µs)		210	415	830	ns
Q_{rr}	Reverse Recovery Charge (I_S = -I_D [Cont.], dI_S/dt = 100A/µs)		4	8.3	16	µC

PACKAGE CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
L_D	Internal Drain Inductance (Measured From Drain Terminal to Center of Die.)		3		nH
L_S	Internal Source Inductance (Measured From Source Terminals to Source Bond Pads)		5		
$V_{Isolation}$	RMS Voltage (50-60 Hz Sinusoidal Waveform From Terminals to Mounting Base for 1 Min.)	2500			Volts
$C_{Isolation}$	Drain-to-Mounting Base Capacitance (f = 1MHz)		35		pF
Torque	Maximum Torque for Device Mounting Screws and Electrical Terminations.			13	in-lbs

①Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve. (Fig.1)

②Pulse Test: Pulse width < 380 µS, Duty Cycle < 2%

③See MIL-STD-750 Method 3471

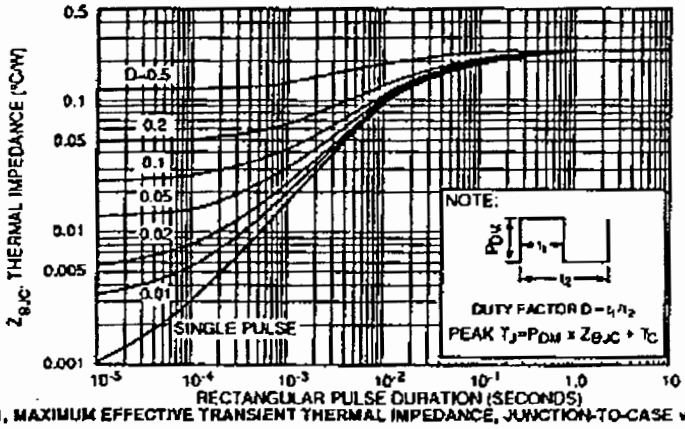


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

APT5010/5012JN

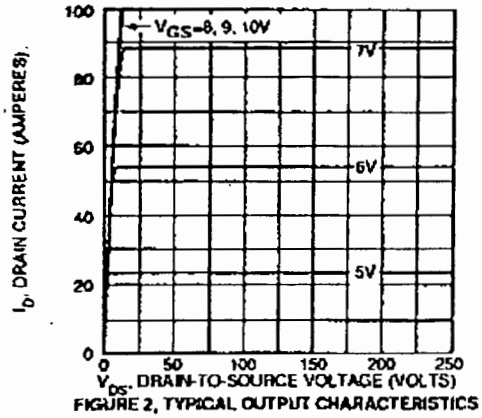


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

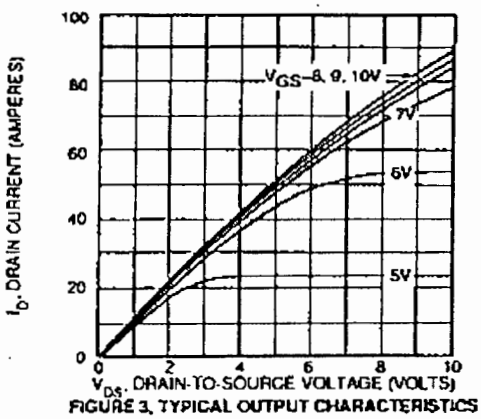


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

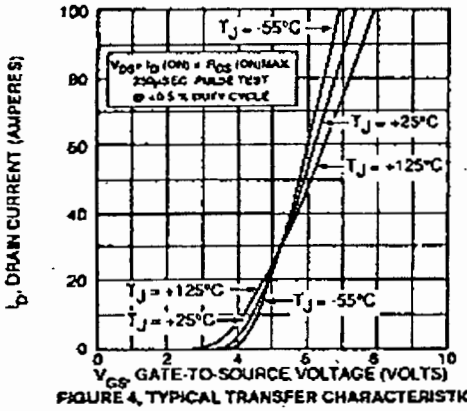


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

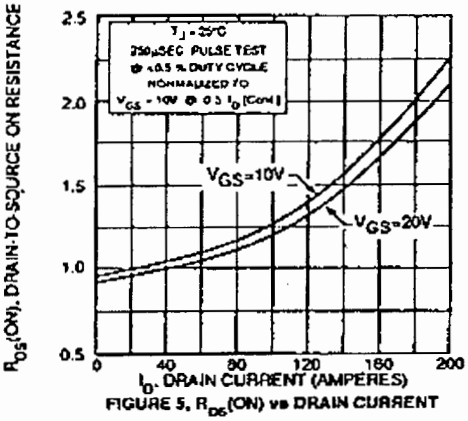


FIGURE 5, R_{DS}(ON) vs DRAIN CURRENT

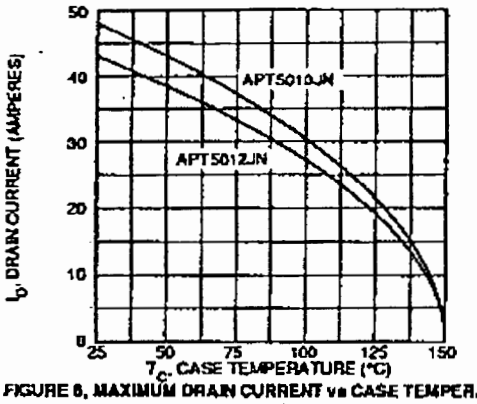


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

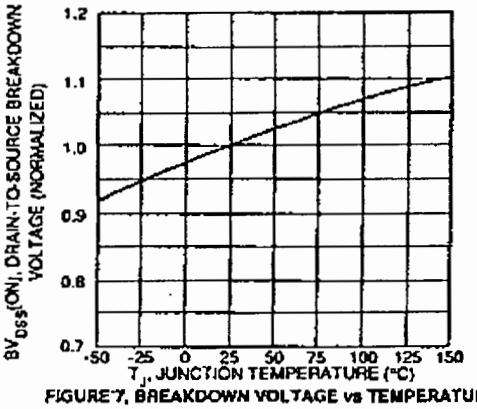


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

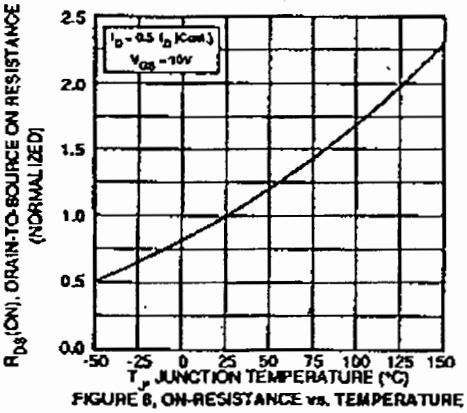


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

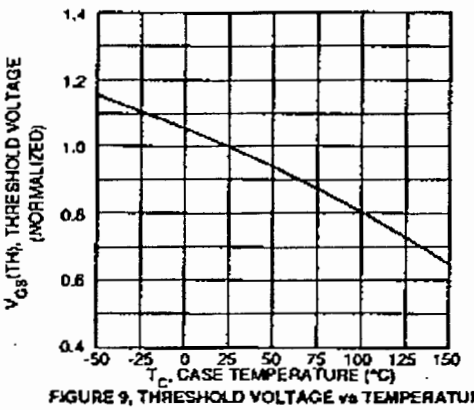


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

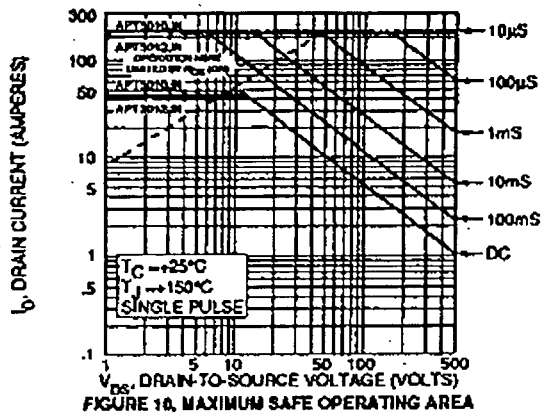


FIGURE 10, MAXIMUM SAFE OPERATING AREA

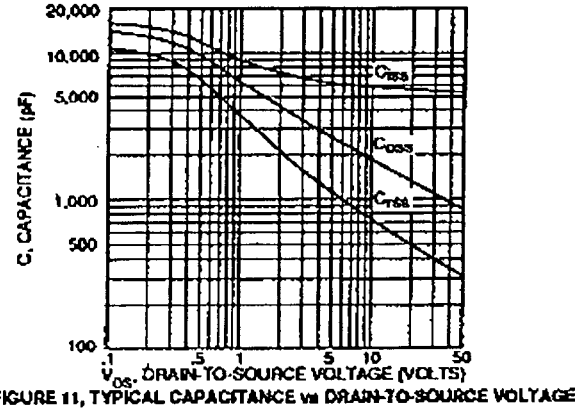


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

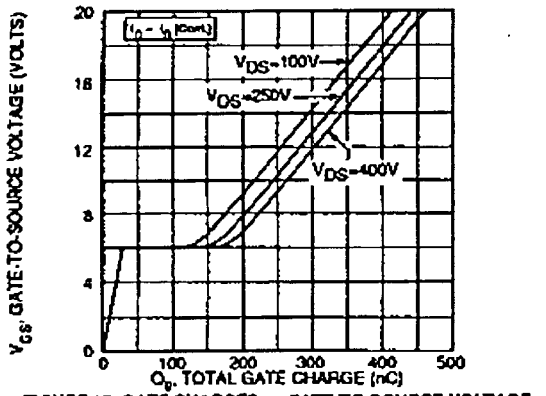


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

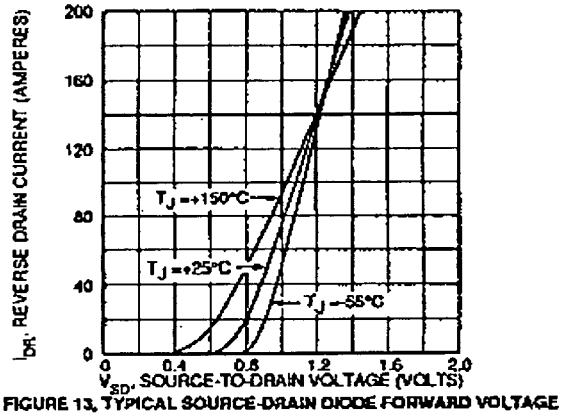
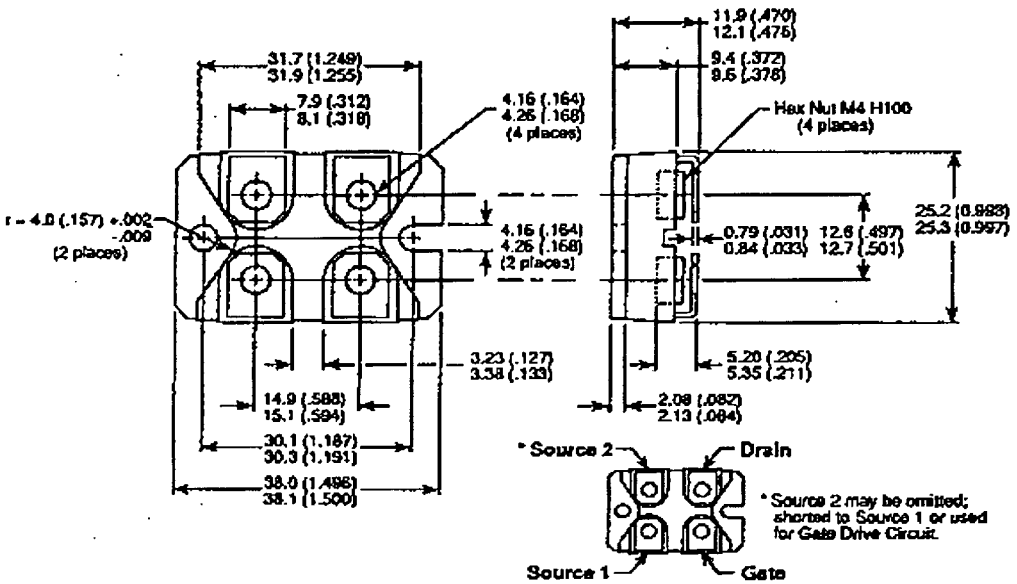


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

SOT-227 Package Outline



Dimensions in Millimeters and (Inches)

Power Factor Controller

FEATURES

- **High Power Factor Over Wide Load Range with Line Current Averaging**
- International Operation Without Switches
- Instantaneous Overvoltage Protection
- Minimal Line Current Dead Zone
- Typical 250µA Startup Supply Current
- Rejects Line Switching Noise
- Synchronization Capability
- Low Quiescent Current: 9mA
- Fast 1.5A Peak Current Gate Driver

APPLICATIONS

- Universal Power Factor Corrected Power Supplies
- Preregulators Up To 1500W

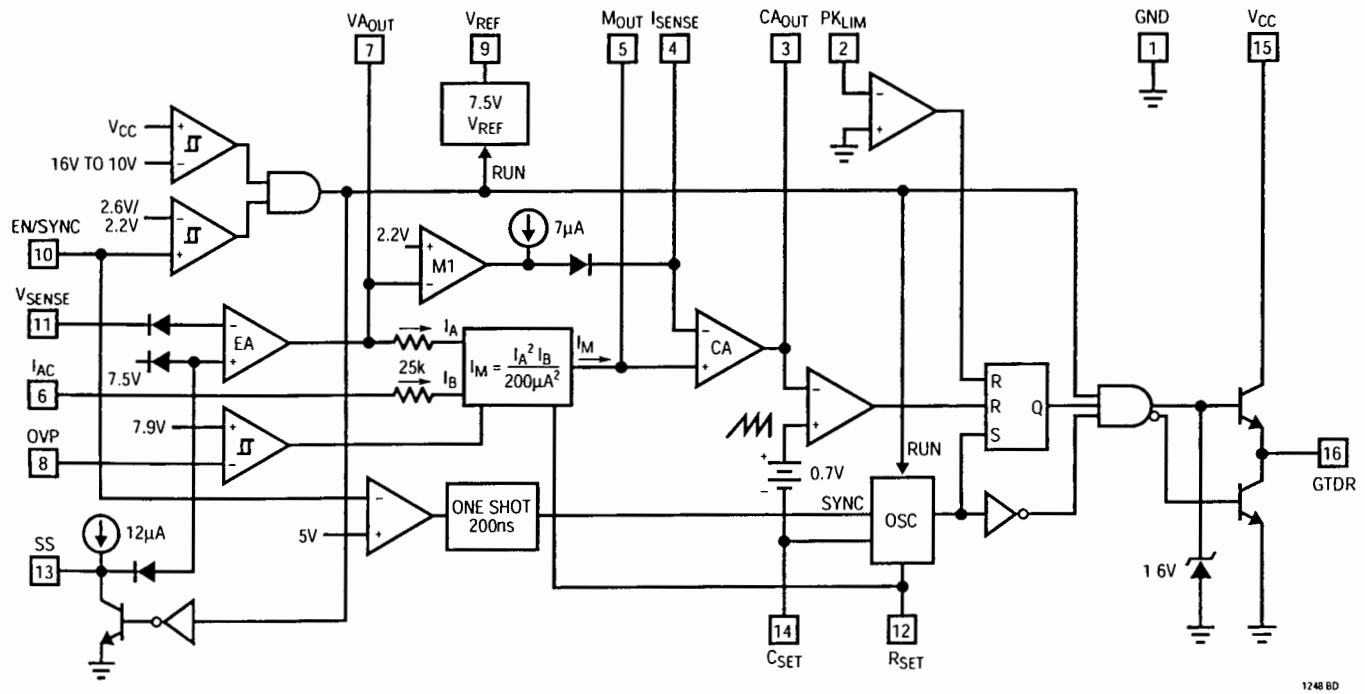
DESCRIPTION

The LT®1248 provides active power factor correction for universal off-line power systems. By using fixed high frequency PWM current averaging, without the need for slope compensation, the LT1248 achieves far lower line current distortion with a smaller magnetic element than systems that use either peak-current detection or zero current switching approaches in both continuous and discontinuous modes of operation.

The LT1248 uses a multiplier that has a square gain function from the voltage amplifier to reduce the AC gain at light output load and thus maintains low line current distortion and high system stability. The LT1248 also provides filtering capability to reject line switching noise which can cause instability when fed into the multiplier. Line current dead zone is minimized with low bias voltage at the current input to the multiplier.

The LT1248 provides many protection features including peak current limiting and overvoltage protection, and can be operated at frequencies as high as 300kHz.

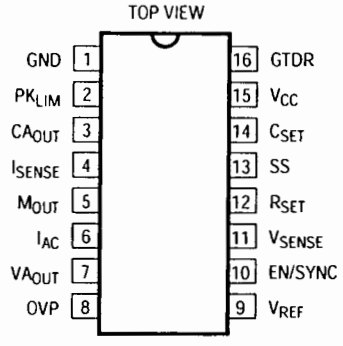
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 27V
GTDR Current Continuous 0.5A
GTDR Output Energy(Per Cycle) 5µJ
I_{AC}, R_{SET}, PK_{LIM} Input Current 20mA
V_{SENSE}, EN/SYNC, OVP Input Voltage ..... V_{MAX}
I_{SENSE}, M_{OUT} Input Current ..... ±5mA
Operating Junction Temperature Range
LT1248C ..... 0°C to 100°C
LT1248I ..... –40°C to 125°C
Thermal Resistance (Junction-to-Ambient)
N Package ..... 100°C/W
S Package ..... 120°C/W
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PLASTIC DIP
S PACKAGE
16-LEAD NARROW PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 120°C/W (S)

ORDER PART NUMBER
LT1248CN
LT1248IN
LT1248CS
LT1248IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

Maximum operating voltage (V_{MAX}) = 25V, V_{CC} = 18V, R_{SET} = 15k to GND, C_{SET} = 1nF to GND, I_{AC} = 100µA, I_{SENSE} = 0V, CA_{OUT} = 3.5V, VA_{OUT} = 5V, OVP = 7.5V, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overall						
Supply Current (V_{CC} in Undervoltage Lockout)	V_{CC} = Lockout Voltage – 0.2V	●		0.25	0.45	mA
Supply Current (Inactive)	EN/SYNC = 0V, $V_{CC} \le V_{MAX}$	●		0.5	1.5	mA
Supply Current, On	11.5V ≤ $V_{CC} \le V_{MAX}$	●		8.5	12.0	mA
V_{CC} Turn-On Threshold (Undervoltage Lockout)		●	15.5	16.5	17.5	V
V_{CC} Turn-Off Threshold		●	9.5	10.5	11.5	V
EN/SYNC Threshold, Rising		●	2.2	2.6	2.85	V
EN/SYNC Threshold Hysteresis				0.40		V
EN/SYNC Input Current	EN/SYNC = 0V 3V ≤ EN/SYNC ≤ 7V	●	–5 –50	–1 –25	5 50	µA µA
Voltage Amplifier						
Voltage Amp Offset Voltage	VA_{OUT} = 3.5V	●	–8		8	mV
Input Bias Current	V_{SENSE} = 0V to 7V	●		–25	–250	nA
Voltage Gain			70	100		dB
Voltage Amp Unity-Gain Bandwidth				3		MHz
Voltage Amp Output High (Internally Clamped)		●	11.3	13.3		V
Voltage Amp Output Low		●		1.1	2	V
Voltage Amp Short-Circuit Current	VA_{OUT} = 0V	●	5	14	30	mA
SS Current	SS = 2.5V	●	5	12	30	µA
Current Amplifier						
Current Amp Offset Voltage		●		±1	±4	mV
I_{SENSE} Bias Current		●		–25	–250	nA
Current Amp Voltage Gain			80	110		dB
Current Amp Unity-Gain Bandwidth				3		MHz
Current Amp Output High		●	7.2	8.5		V
Current Amp Output Low		●		1.1	2	V

ELECTRICAL CHARACTERISTICS

Maximum operating voltage (V_{MAX}) = 25V, V_{CC} = 18V, R_{SET} = 15k to GND, C_{SET} = 1nF to GND, I_{AC} = 100µA, I_{SENSE} = 0V, CA_{OUT} = 3.5V, VA_{OUT} = 5V, OVP = 7.5V. No load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Amplifier						
Current Amp Short-Circuit Current	CA_{OUT} = 0V	●	5	14	30	mA
Input Range, I_{SENSE}, M_{OUT} (Linear Operation)		●	–0.3		1	V
Reference						
Reference Output Voltage	I_{REF} = 0mA, T_A = 25°C		7.39	7.50	7.60	V
V_{REF} Load Regulation	–5mA < I_{REF} < 0mA			5		mV
V_{REF} Line Regulation	11.5V < V_{CC} < V_{MAX}	●	–20	5	20	mV
V_{REF} Short-Circuit Current	V_{REF} = 0V	●	12	28	50	mA
V_{REF} Worst Case	Load, Line, Temperature	●	7.32	7.5	7.68	V
Current Limit						
PK_{LIM} Offset Voltage		●	–15		15	mV
PK_{LIM} Input Current	PK_{LIM} = –0.1V	●		–50	–100	µA
PK_{LIM} to GTDR Propagation Delay	PK_{LIM} Falling from 50mV to –50mV			400		ns
Multiplier						
Multiplier Output Current	I_{AC} = 100µA, R_{SET} = 15k			35		µA
Multiplier Output Current Offset	R_{AC} = 1M from I_{AC} to GND	●		–0.05	–0.5	µA
Multiplier Maximum Output Current	I_{AC} = 450µA, R_{SET} = 15k, VA_{OUT} = 7V, M_{OUT} = 0V	●	–286	–260	–235	µA
Multiplier Gain Constant (Note 1)				0.035		V^{-2}
I_{AC} Input Resistance	I_{AC} from 50µA to 1mA		15	25	35	kΩ
Oscillator						
Oscillator Frequency	R_{SET} = 15k, C_{SET} = 1000pF	●	85	100	115	kHz
	R_{SET} = 15k, C_{SET} = 1500pF	●	58	68	78	kHz
C_{SET} Ramp Peak-to-Peak Amplitude			4.35	4.7	5.0	V
C_{SET} Ramp Valley Voltage			1.25	1.4	1.55	V
Synchronization Pulse Threshold on EN/SYNC Pin	Pulse Low = 3.5V, High = 7V, Width > 200ns		4.5	5.6	6.5	V
Synchronization Frequency Range	R_{SET} = 15k, C_{SET} = 1000pF	●	1.2		1.6	· f_{NOM}
Overvoltage Comparator						
Comparator Trip Voltage Ratio (V_{TRIP}/V_{REF})		●	1.04	1.05	1.06	
Hysteresis				0.35		V
OVP Bias Current	OVP = 7.5V	●		–50	–250	nA
OVP Propagation Delay				100		ns
Gate Driver						
Max GTDR Output Voltage	0mA Load, 18V < V_{CC}	●	12	15	17.5	V
GTDR Output High	–200mA Load, 11.5V ≤ V_{CC} ≤ 15V	●	V_{CC} – 3.0			V
GTDR Output Low (Device Unpowered)	V_{CC} = 0V, 50mA Load (Sinking)	●		0.9	1.5	V
GTDR Output Low (Device Active)	200mA Load (Sinking)	●		0.5	1	V
	10mA Load	●		0.2	0.4	V
Peak GTDR Current	10nF from GTDR to GND			2		A
GTDR Rise and Fall Time	1nF from GTDR to GND			25		ns
GTDR Max Duty Cycle			90	96		%

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Multiplier Gain Constant: $K = \frac{I_M}{I_{AC}\,(VA_{OUT} - 2)^2}$

Power Factor Controllers (continued)

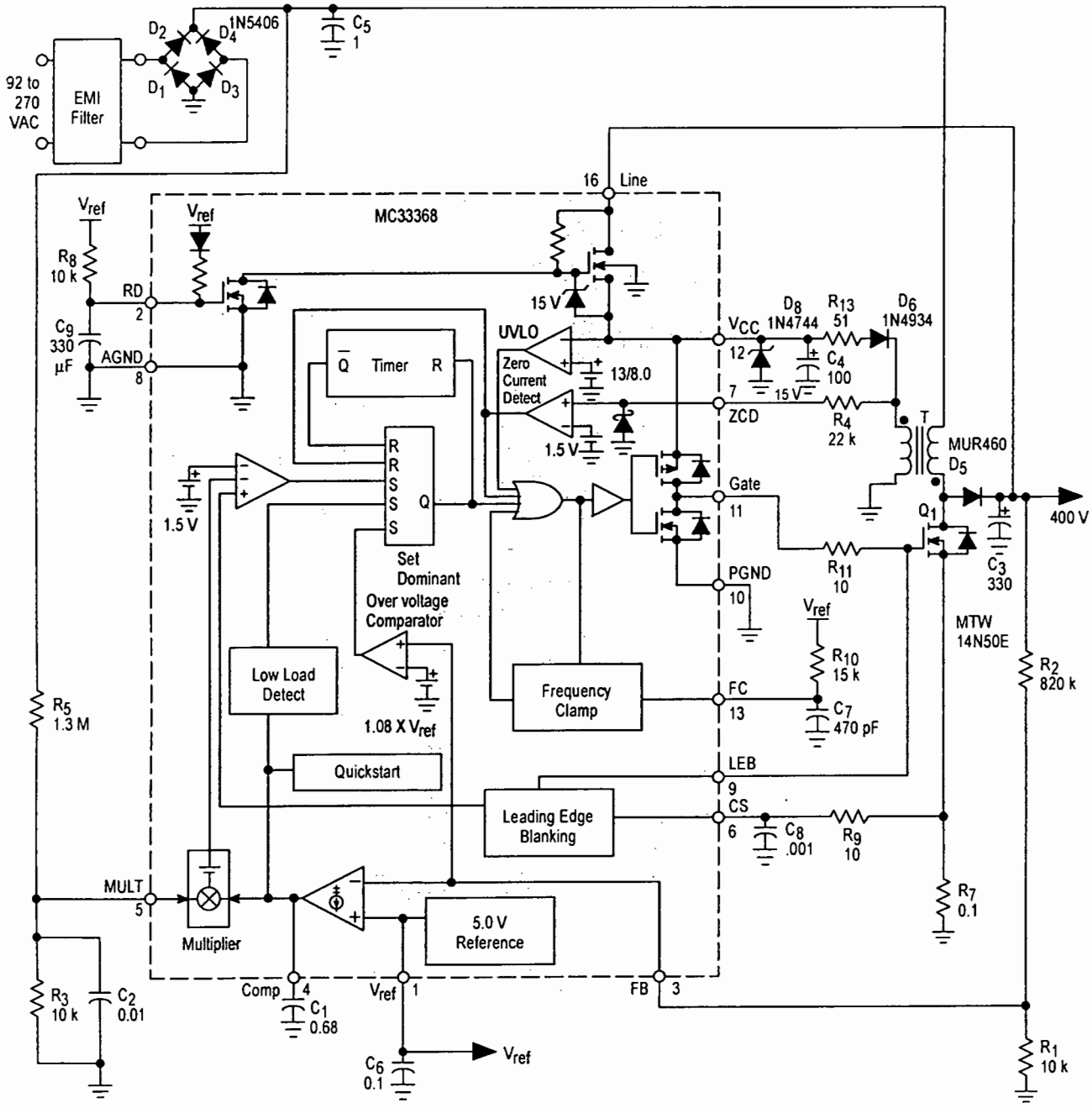
MC33368D

T_A = –25° to +125°C, Case 751K

The MC33368 is an active power factor controller that functions as a boost preconverter in off–line power supply applications. MC33368 is optimized for low power, high density power supplies requiring minimum board area, reduced component count, and low power dissipation. The narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

The MC33368 features a watchdog timer to initiate output switching, a one quadrant multiplier to force the line current to follow the instantaneous line voltage, a zero current detector to ensure critical conduction operation, a transconductance error amplifier, a current sensing comparator, a 5.0 V reference, an undervoltage lockout (UVLO) circuit which monitors the V_{CC} supply voltage, and a CMOS driver for driving MOSFETs. The MC33368 also includes a programmable output switching frequency clamp. Protection features include an output overvoltage comparator to minimize overshoot, a restart delay timer, and cycle–by–cycle current limiting.

- Lossless Off–Line Startup
- Output Overvoltage Comparator
- Leading Edge Blanking (LEB) for Noise Immunity
- Watchdog Timer to Initiate Switching
- Restart Delay Timer



TR Module

Unit in mm

ilicon N Channel IGBT

gh Power Switching Applications

otor Control Applications

atures

High input impedance

High speed: t_f = 0.30μs (Max.) (I_C = 75A)

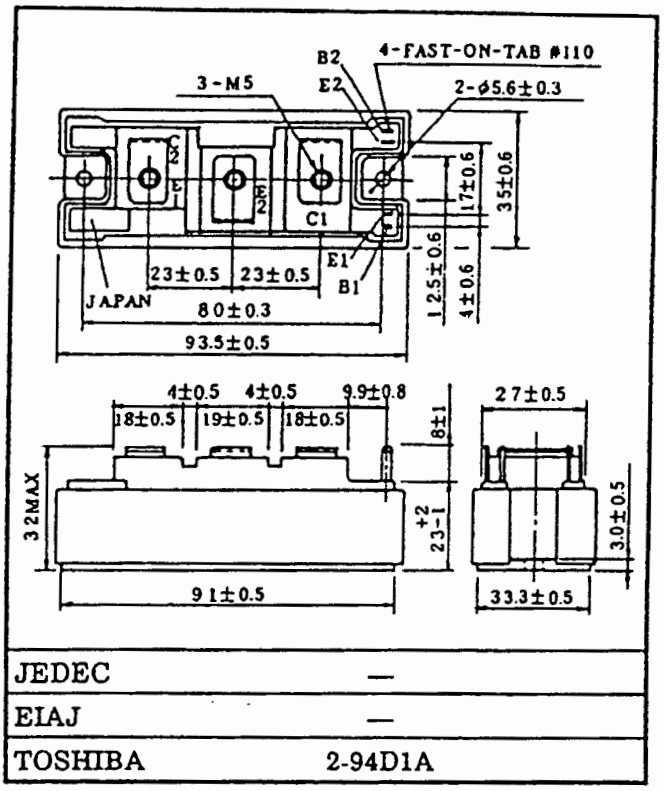
t_{rr} = 0.15μs (Max.) (I_F = 75A)

Enhancement mode

The electrodes are isolated from case

Includes a complete half bridge card in one package

Low saturation voltage $V_{CE\ (sat)}$ = 2.70V (Max.) (I_C = 75A)



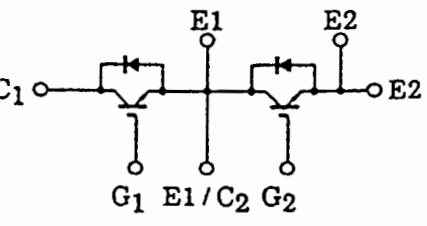
JEDEC	—
EIAJ	—
TOSHIBA	2-94D1A

Weight : 202g (Typ.)

aximum Ratings (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
ollector-Emitter Voltage		V_{CES}	600	V
ate-Emitter Voltage		V_{GES}	±20	V
ollector Current	DC	I_C	75	A
	1ms	I_{CP}	150	
orward Current	DC	I_F	75	A
	1ms	I_{FM}	150	
ollector Power issipation (Tc = 25°C)		P_C	390	W
unction Temperature		T_j	150	°C
torage Temperature Range		T_{stg}	-40 ~ 125	°C
solation Voltage		V_{Isol}	2500 (AC 1 min.)	V
crew Torque (Terminal/Mounting)		—	3/3	N ¥ m

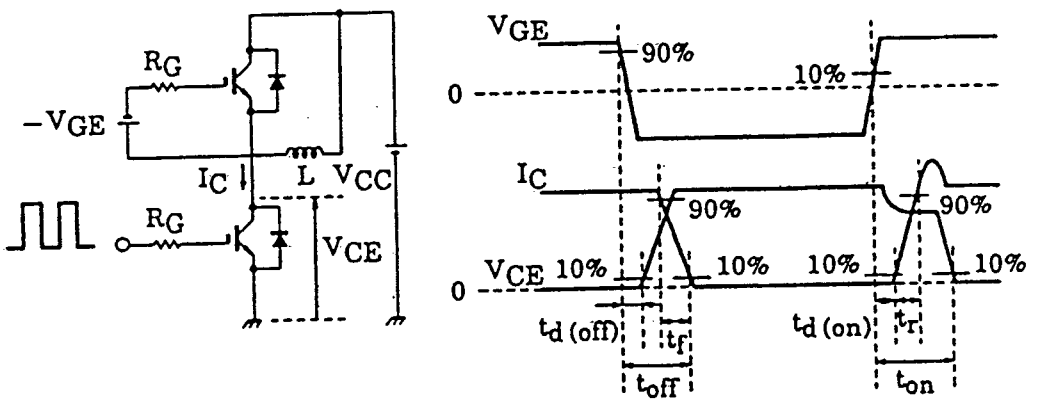
quivalent Circuit



Electrical Characteristics (Ta = 25°C)

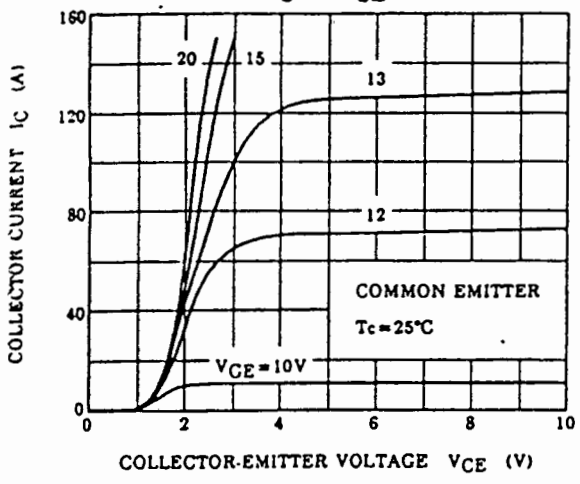
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GES}	V_{GE} = ± 20V, V_{CE} = 0	—	—	± 500	nA
Collector Cut-off Current		I_{CES}	V_{CE} = 600V, V_{GE} = 0	—	—	1.0	mA
Gate-Emitter Cut-off Voltage		$V_{GE\ (off)}$	I_C = 7.5mA, V_{CE} = 5V	5.0	7.0	8.0	V
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$	I_C = 75A, V_{GE} = 15V	—	2.10	2.70	V
Input Capacitance		C_{ies}	V_{CE} = 10V, V_{GE} = 0, f = 1MHz	—	7100	—	pF
Switching Time	Turn-on Delay Time	$t_{d\ (on)}$	Inductive Load V_{CC} = 300V I_C = 75A V_{GE} = ± 15V R_G = 18Ω (Note 1)	—	0.08	0.16	µs
	Rise Time	t_r		—	0.12	0.24	
	Turn-on Time	t_{on}		—	0.40	0.80	
	Turn-off Delay Time	$t_{d\ (off)}$		—	0.20	0.40	
	Fall Time	t_f		—	0.15	0.30	
	Turn-off Time	t_{off}		—	0.50	1.00	
Forward Voltage		V_F	I_F = 75A, V_{GE} = 0	—	2.10	2.80	V
Reverse Recovery Time		t_{rr}	I_F = 75A, V_{GE} = -10V di/dt = 100A/µs	—	0.08	0.15	µs
Thermal Resistance		$R_{th\ (j-c)}$	Transistor	—	—	0.32	°C/W
			Diode	—	—	0.69	

Note 1 Switching Time Test Circuit & Timing Chart.

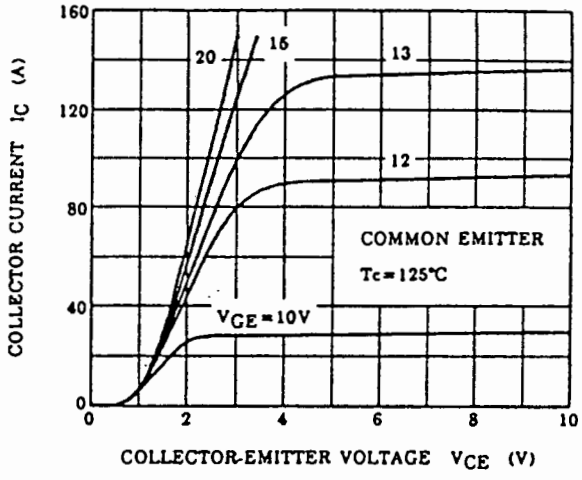


Note 2 Silicone Grease is Applied.

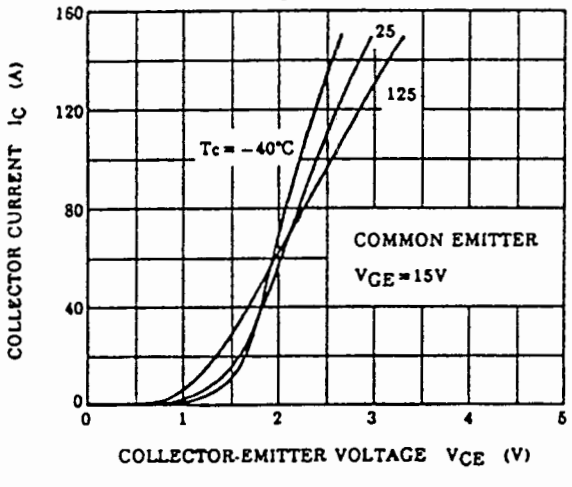
I_C – V_{CE}



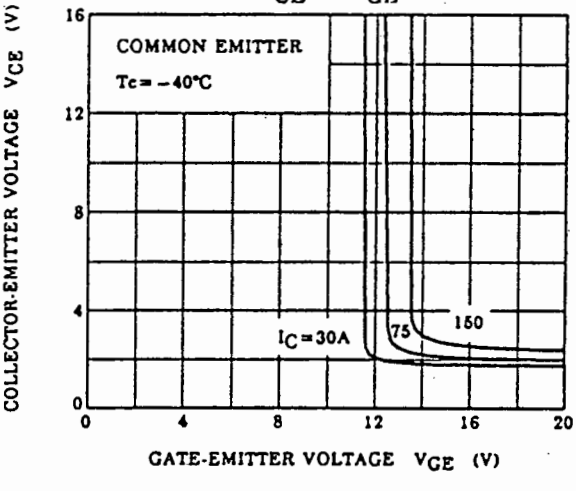
I_C – V_{CE}



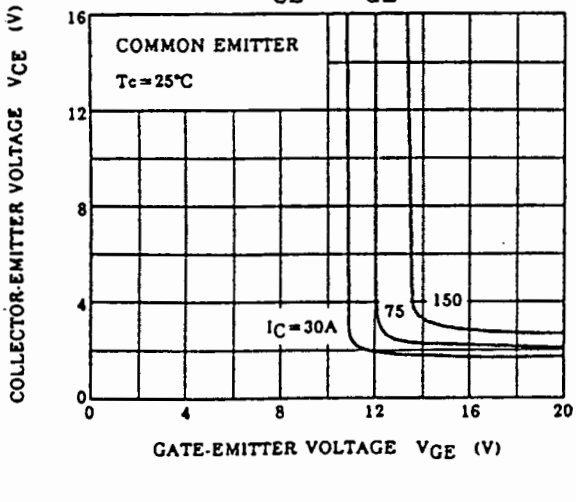
I_C – V_{CE}



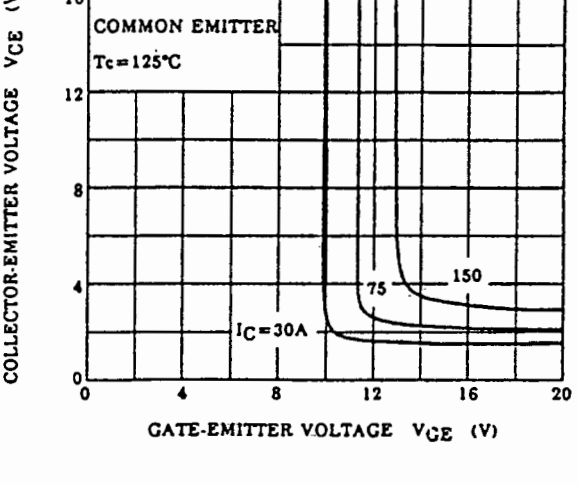
V_{CE} – V_{GE}



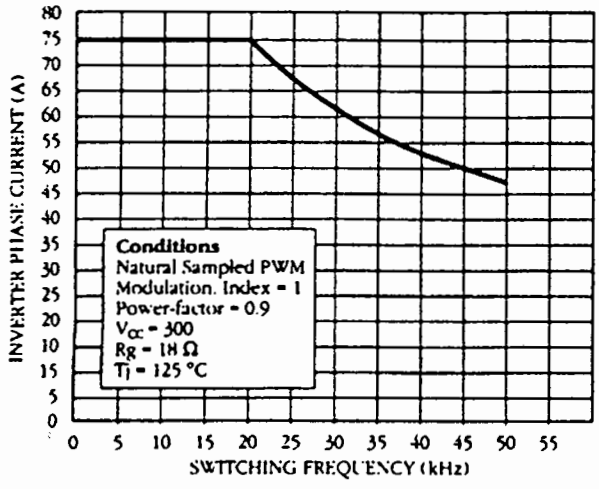
V_{CE} – V_{GE}

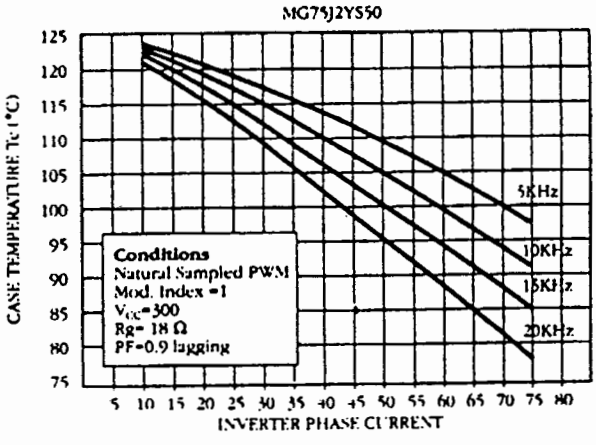


V_{CE} – V_{GE}

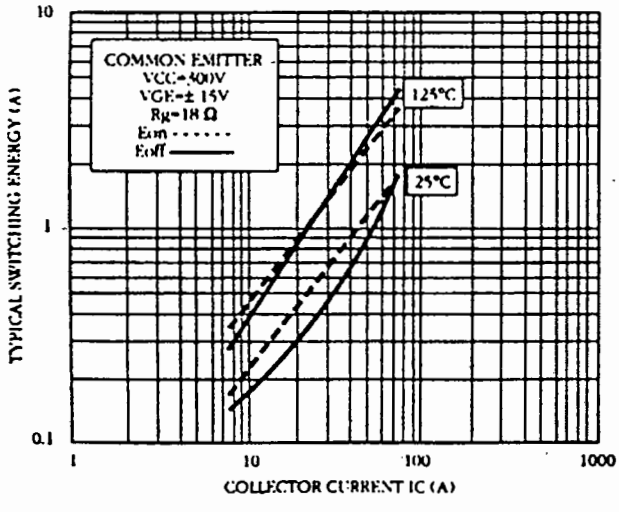


TYPICAL INVERTER PHASE CURRENT AT TCASE = 80 °C

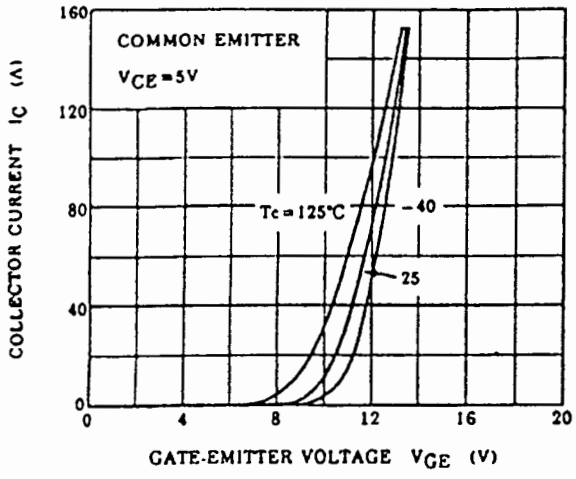




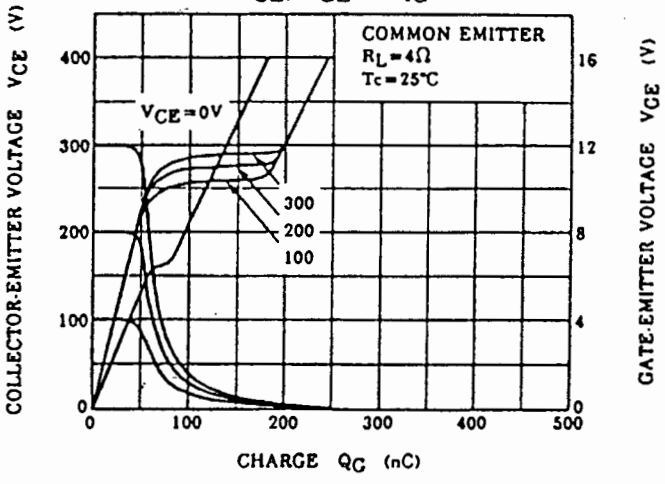
TYPICAL SWITCHING ENERGY (IC)



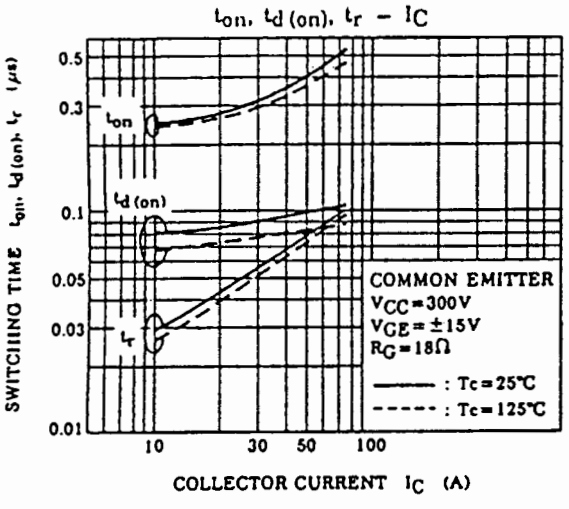
I_C – V_{GE}



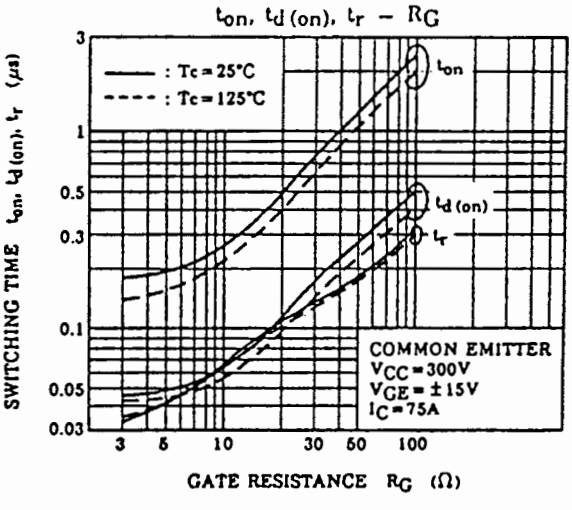
V_{CE}, V_{GE} – Q_G



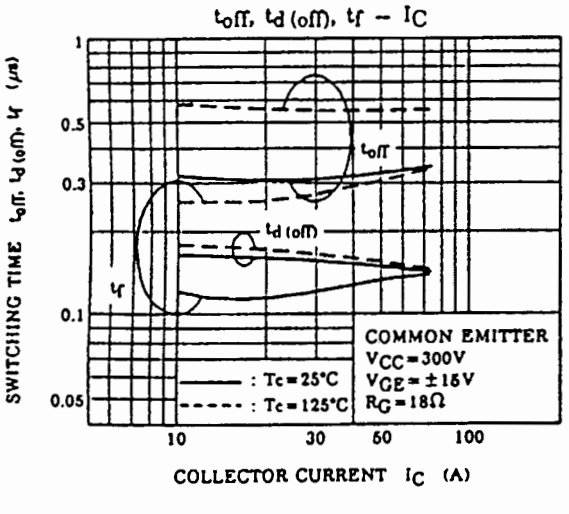
t_{on}, $t_{d(on)}$, t_r – I_C



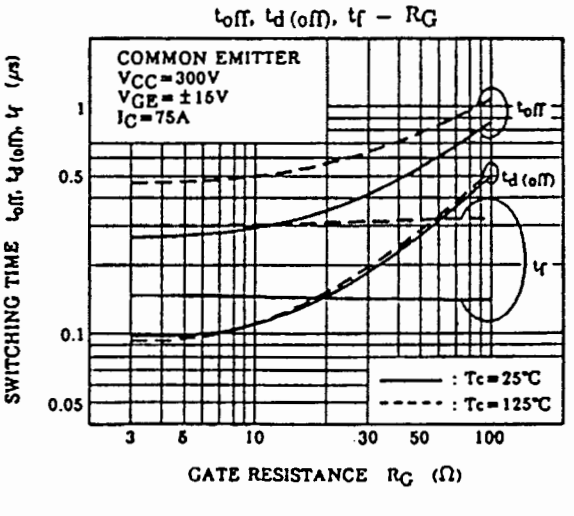
t_{on}, $t_{d(on)}$, t_r – R_G



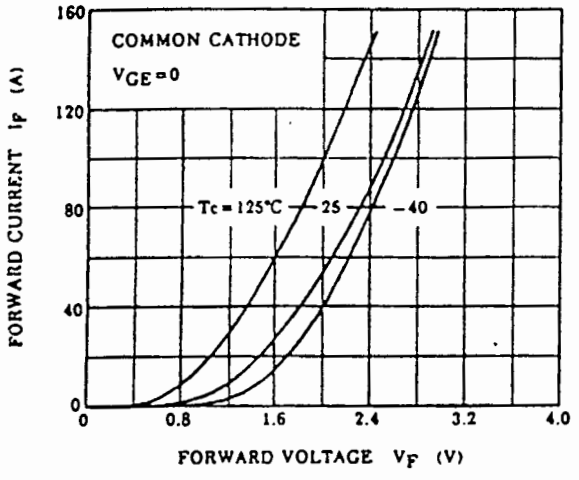
t_{off}, $t_{d(off)}$, t_f – I_C



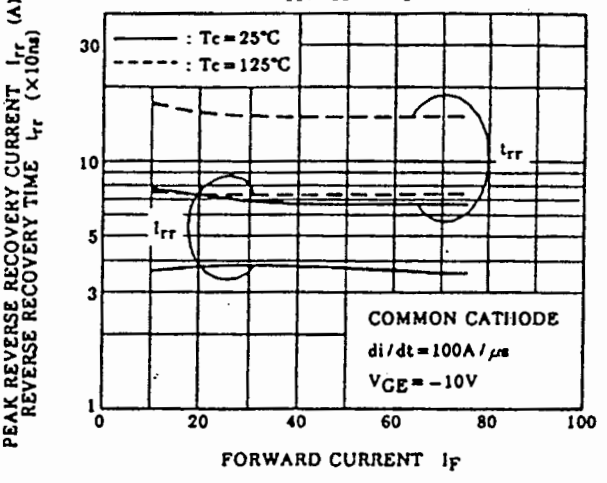
t_{off}, $t_{d(off)}$, t_f – R_G



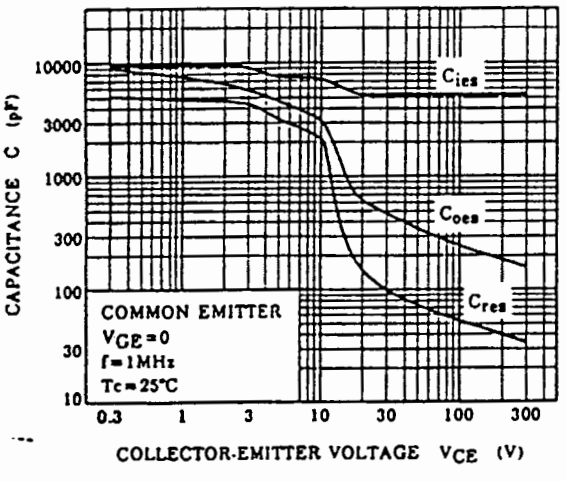
$I_F - V_F$



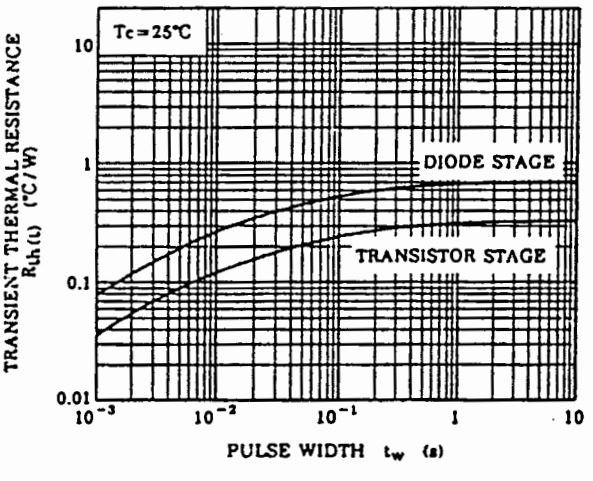
$t_{rr}, I_{rr} - I_F$



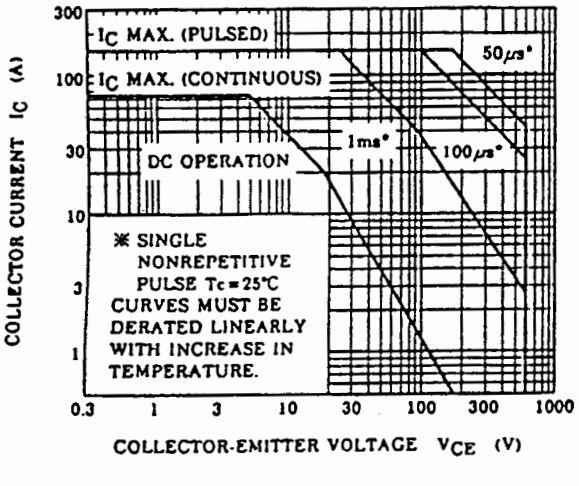
$C - V_{CE}$



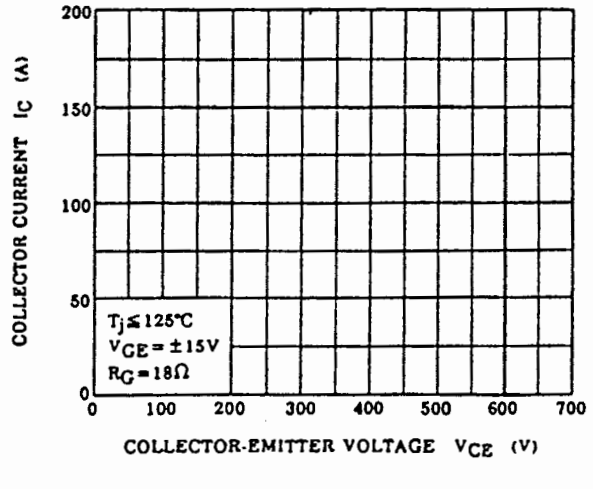
$R_{th(t)} - t_w$



SAFE OPERATING AREA



REVERSE BIAS SOA

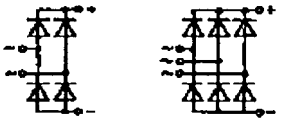


SEMIKRON

Power Bridge Rectifiers
SKB 50
SKD 50

V_{RSM} V_{RRM}	I_D (T_{case} = ...) 50 A (64 °C)		50 A (92 °C)	
V	Types	R_{thJC} Ω	Types	R_{thJC} Ω
200	SKB 50/02 A3	0,1	SKD 50/02 A3	0,1
400	SKB 50/04 A3	0,3	SKD 50/04 A3	0,2
800	SKB 50/08 A3	0,4	SKD 50/08 A3	0,4
1200	SKB 50/12 A3	0,6	SKD 50/12 A3	0,6
1600	SKB 50/16 A3	0,8	SKD 50/16 A3	0,8

Symbol	Conditions		SKB 50	SKD 50
I_D	T_{amb} = 35 °C;	P1/120 F	48 A	60 A
	T_{amb} = 45 °C;	isolated[1]	10 A	10 A
		chassis[2]	20 A	22 A
		P1/120	34 A	40 A
	T_{amb} = 35 °C;	P1/120 F	40 A	60 A
	T_{amb} = 45 °C;	isolated[1]	8 A	10 A
		chassis[2]	16 A	22 A
		P1/120	29 A	40 A
I_N	T_{amb} = 35 °C;	P1/120 F	40 A	48 A
	T_{amb} = 45 °C;	isolated[1]	8 A	8 A
		chassis[2]	16 A	18 A
		P1/120	27 A	32 A
I_{NCL}	T_{amb} = 35 °C;	P1/120 F	32 A	48 A
	T_{amb} = 45 °C;	isolated[1]	6,5 A	8 A
		chassis[2]	13 A	18 A
		P1/120	23 A	32 A
I_{FSM}	T_{vj} = 25 °C, 10 ms		750 A	
	T_{vj} = 150 °C, 10 ms		600 A	
i^2t	T_{vj} = 25 °C, 8,3...10 ms		2800 A^2s	
	T_{vj} = 150 °C, 8,3...10 ms		1800 A^2s	
V_F	T_{vj} = 25 °C; I_F = 150 A		1,6 V	
$V_{(TO)}$	T_{vj} = 150 °C		0,85 V	
r_T	T_{vj} = 150 °C		8 mΩ	
I_{RD}	T_{vj} = 25 °C; V_{RD} = V_{RRM}		1 mA	
	T_{vj} = 150 °C; V_{RD} = V_{RRM}		10 mA	
t_{rr}	T_{vj} = 25 °C		typ. 10 µs	
f_G			2000 Hz	
R_{thJC}	total		0,65 °C/W	0,45 °C/W
R_{thCH}	total		0,06 °C/W	0,06 °C/W
	T_{amb} = 35 °C;	P1/120 F	0,9 °C/W	0,7 °C/W
		isolated[1]	5,7 °C/W	5,5 °C/W
		chassis[2]	2,5 °C/W	2,3 °C/W
		P1/120	1,3 °C/W	1,1 °C/W
T_{vj}			− 40...+ 150 °C	
T_{stg}			− 55...+ 150 °C	
V_{isol}	a.c. 50 Hz; r.m.s.		2500 V~	
RC	P_R = 1 W		0,1 µF+50 Ω	
Fu			50 A	
M_1	case to heatsink	SI units/	5 Nm/44 lb. in. ± 15 %	
M_2	busbars to terminals	US units	3 Nm/26 lb. in. ± 15 %	
w			250 g	
Case			G 14	G 15



SKB SKD

Features
- Isolated metal case with screw terminals
- Blocking voltage to 1600 V
- High surge current
- SKB = single phase bridge rectifier
  SKD = three phase bridge rectifier
- Easy chassis mounting

Typical Applications
- Single and three phase rectifiers for power supplies
- Input rectifiers for variable frequency drives
- Rectifiers for DC motor field supplies
- Battery charger rectifiers

[1] Freely suspended or mounted on an insulator
[2] Mounted on a painted metal sheet of min. 250 x 250 x 1 mm

INTEGRATED CIRCUITS

UNITRODE

UC1854A/B
UC2854A/B
UC3854A/B

Enhanced High Power Factor Preregulator

FEATURES

- Controls Boost PWM to Near Unity Power Factor
- Limits Line Current Distortion To <3%
- World-Wide Operation Without Switches
- Accurate Power Limiting
- Fixed Frequency Average Current Mode Control
- High Bandwidth (5MHz), Low Offset Current Amplifier
- Integrated Current and Voltage Amp Output Clamps
- Multiplier Improvements: Linearity, 500mV VAC Offset (eliminates extemal resistor), 0-5V Multout Common Mode Range
- V_{REF} "GOOD" Comparator
- Faster and Improved Accuracy ENABLE Comparator
- UVLO Threshold Options (16/10V / 10.5/10V)
- 300µA Startup Supply Current

	UVLO Turn on	UVLO Turn off
UC1854A	16V	10V
UC1854B	10.5V	10V

DESCRIPTION

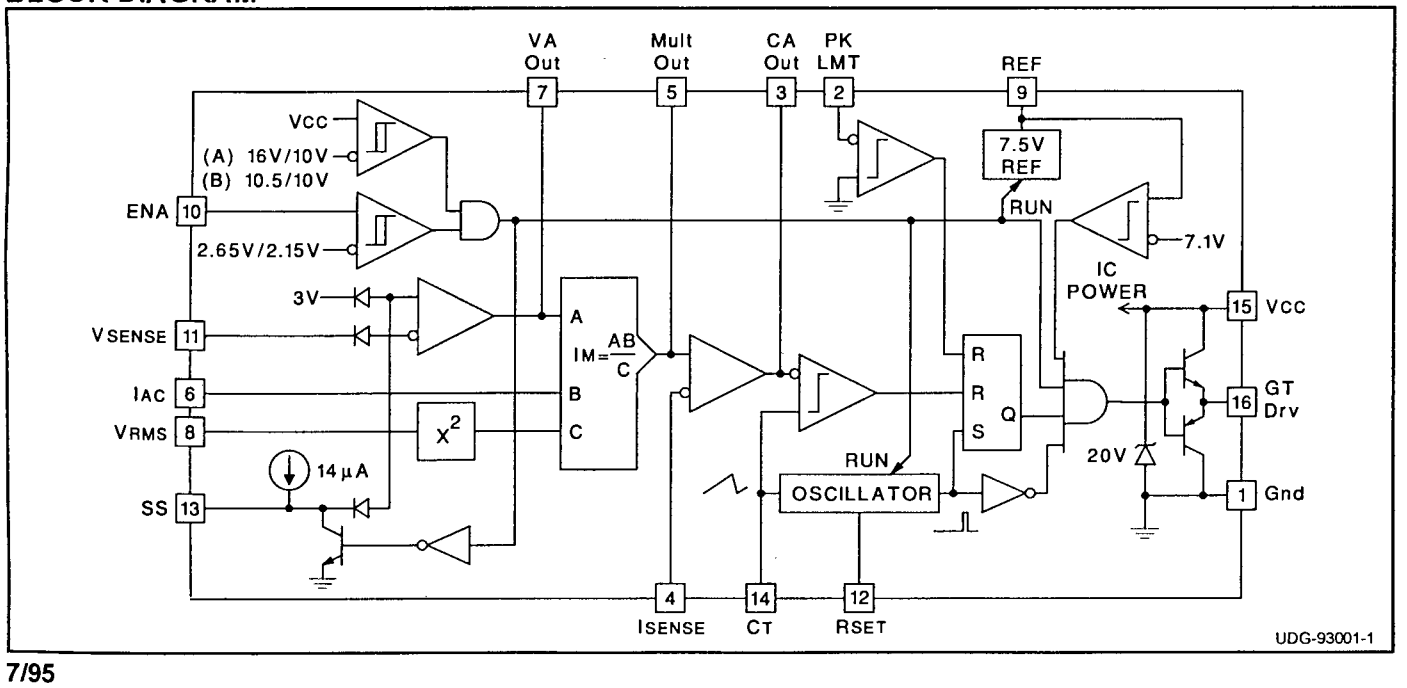
The UC1854A/B products are pin compatible enhanced versions of the UC1854. Like the UC1854, these products provide all of the functions necessary for active power factor corrected prer egulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage. To do this the UC1854A/B uses average current mode control. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control.

The UC1854A/B products improve upon the UC1854 by offering a wide bandwidth, low offset Current Amplifier, a faster responding and improved accuracy enable comparator, a V_{REF} "good" comparator, UVLO threshold options (16/10V for offline, 10.5/10V for startup from an auxiliary 12V regulator), lower startup supply current, and an enhanced multiply/divide circuit. New features like the amplifier output clamps, improved amplifier current sinking capability, and low offset VAC pin reduce the external component count while improving performance. Improved common mode input range of the Multiplier output/Current Amp input allow the designer greater flexibility in choosing a method for current sensing. Unlike its predecessor, R_{SET} controls only oscillator charging current and has no effect on clamping the maximum multiplier output current. This current is now clamped to a maximum of 2 * I_{AC} at all times which simplifies the design process and provides foldback power limiting during brownout and extreme low line conditions.

A 1% 7.5V reference, fixed frequency oscillator, PWM, Voltage Amplifier with softstart, line voltage feedforward (V_{RMS} squarer), input supply voltage clamp, and over current comparator round out the list of features.

Available in the 16 pin N, DW, and J and 20 pin L and Q packages.

BLOCK DIAGRAM



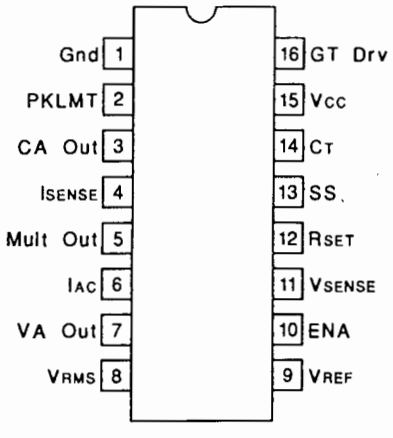
ABSOLUTE MAXIMUM RATINGS

Supply Voltage Vcc 22V
GT Drv Current, Continuous 0.5A
GT Drv Current, 50% Duty Cycle 1.5A
Input Voltage, VSENSE, VRMS 11V
Input Voltage, ISENSE, Mult Out 11V
Input Voltage, PKLMT 5V
Input Current, RSET, IAC, PKLMT, ENA 10mA
Power Dissipation 1W
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

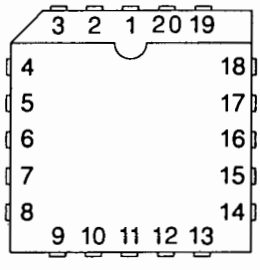
Note 1: All voltages with respect to Gnd (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: ENA imput is internally clamped to approximately 10V.
Note 4: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

DIL–16 & SOIC-16
(Top View)
J, N & DW Packages



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Gnd	2
PKLMT	3
CA Out	4
ISENSE	5
N/C	6
Mult Out	7
IAC	8
VA Out	9
VRMS	10
N/C	11
VREF	12
ENA	13
VSENSE	14
RSET	15
N/C	16
SS	17
CT	18
VCC	19
GT Drv	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, Vcc=18V, RT=8.2k, CT=1.5nF, PKLMT=1V, VRMS=1.5V, IAC=100µA, ISENSE=0V, CA Out=3.5V, VA Out=5V, VSENSE=3V, –55°C<TA<125°C for the UC1854A/B, –40°C<TA<85°C for the UC2854A/B, and 0°C<TA<70°C for the UC3854A/B, and TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL					
Supply Current, Off	CAO, VAO = 0V, Vcc = UVLO - 0.3V		250	400	µA
Supply Current, On			12	18	mA
Vcc Turn-On Threshold	UC1854A		16	17.5	V
	UC1854B		10.5	11.2	V
Vcc Turn-Off Threshold	UC1854A / B	9	10		V
Vcc Clamp	I(Vcc) = Icc(on) + 5mA	18	20	22	V
VOLTAGE AMPLIFIER					
Input Voltage		2.9	3.0	3.1	V
VSENSE Bias Current		–500	–25	500	nA
Open Loop Gain	VOUT = 2 to 5V	70	100		dB
VOUT High	ILOAD = –500µA		6		V
VOUT Low	ILOAD = 500µA		0.3	0.5	V
Output Short Circuit Current	VOUT = 0V		1.5	3.5	mA
Gain Bandwidth Product	Fin = 100kHz, 10mV p-p, (Note 1)		1		mHz

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, V_{CC}=18V, R_T=8.2k, C_T=1.5nF, PKLMT=1V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=3V, –55°C<T_A<125°C for the UC1854A/B, –40°C<T_A<85°C for the UC2854A/B, and 0°C<T_A<70°C for the UC3854A/B, and T_A=T_J.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT AMPLIFIER						
Input Offset Voltage	V_{CM} = 0V	T_A = +25°C	–4		0	mV
		OverTemp	–5.5		0	mV
Input Bias Current(sense)	V_{CM} = 0V		–500		500	nA
Open Loop Gain	V_{CM} = 0V, V_{OUT} = 2 to 6V		80	110		dB
V_{OUT} High	I_{LOAD} = –500µA			8		V
V_{OUT} Low	ILOAD = 500µA			0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V			1.5	3.5	mA
Common Mode Range			–0.3		5	V
Gain Bandwidth Product	Fin = 100kHz, 10mV p-p, (Note 1)		3	5		mHz
REFERENCE						
Output Voltage	I_{REF} = 0mA, T_A = 25°C		7.4	7.5	7.6	V
	I_{REF} = 0mA		7.35	7.5	7.65	V
Load Regulation	I_{REF} = 1 to 10mA		0	8	20	mV
Line Regulation	V_{CC} = 12 to 18V		0	14	25	mV
Short Circuit Current	V_{REF} = 0V		25	35	45	mA
OSCILLATOR						
Initial Accuracy	T_A = 25°C		85	100	115	kHz
Voltage Stability	V_{CC} = 12 to 18V			1		%
Total Variation	Line, Temp		80		120	kHz
Ramp Amplitude (p-p)			4.9		5.9	V
Ramp Valley Voltage			0.8		1.3	V
ENABLE / SOFTSTART / CURRENT LIMIT						
Enable Threshold			2.5	2.65	2.8	V
Enable Hysteresis	V_{FAULT} = 2.5V			500	600	mV
Enable Input Bias Current	V_{ENABLE} = 0V			–2	–5	µA
Propagation Delay to Disable	Enable Overdrive = –100mV,(Note 1)			300		ns
SS Charge Current	$V_{SOFTSTART}$ = 2.5V		10	14	24	
PKLMT Offset Voltage			–15		15	mV
PKLMT Input Current	V_{PKLMT} = –0.1V		–200	–100		µA
PKLMT Propagation Delay	(Note 1)			150		ns
MULTIPLIER						
Output Current - I_{AC} Limited	I_{AC}=100µA, V_{RMS} = 1V, R_{SET} = 10k		–220	–200	–170	µA
Output Current - Zero	I_{AC}=0µA, R_{SET} = 10k		–2.0	–0.2	2.0	µA
Output Current - Power Limited	V_{RMS} = 1.5V, Va = 6V		–230	–200	–170	µA
Output Current	V_{RMS} = 1.5V, Va = 2V			–22		µA
	V_{RMS} = 1.5V, Va = 5V			–156		µA
	V_{RMS} = 5V, Va = 2V			–2		µA
	V_{RMS} = 5V, Va = 5V			–14		µA
Gain Constant	(Note 2) V_{RMS} = 1.5V, T_J = 25°C, Va = 6V		–1.1	–1.0	–0.9	A/A

Note 1: Guaranteed by design, not 100% tested in production.

Note 2: Gain constant (K) $= \dfrac{I_{AC} \times (Va - 1.5V)}{V_{RMS}^{\,2} \times I_{MO}}$

Appendix E : Schematics Diagrams

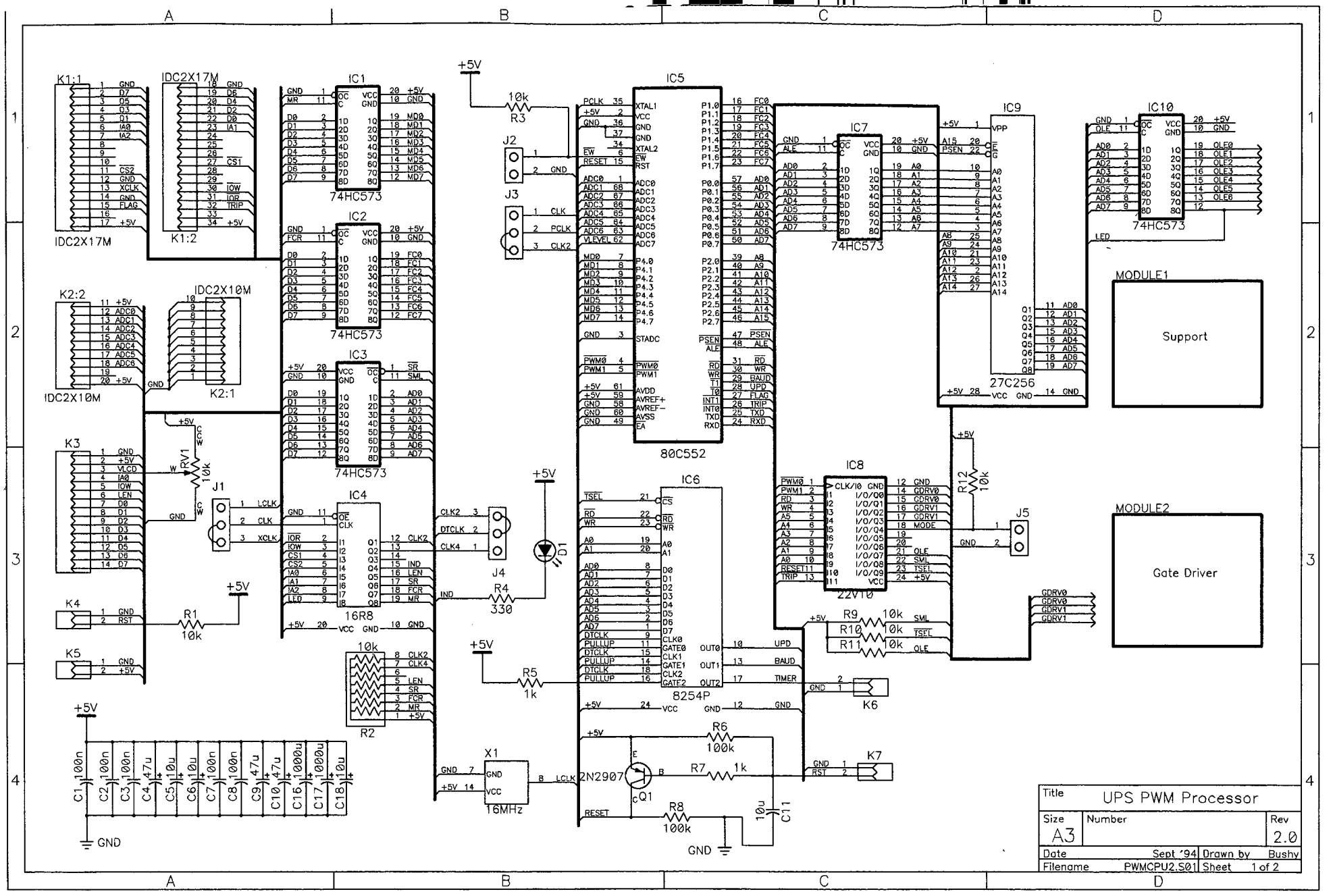
All schematics and printed circuit boards were created using Tango V2.11 .

Controller schematics

- Inverter - 80C552 microcontroller
- Inverter - Interface drivers
- Inverter - SKHI21 IGBT gate driver
- Inverter - Analog interface
- UC3854 power factor controller

Power schematics

- Boost converter
- IGBT bridge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Rev 2.0
Date Sept '94
Drawn by Bushy
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Sheet 1 of 2
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Support
MODULE2
Gate Driver
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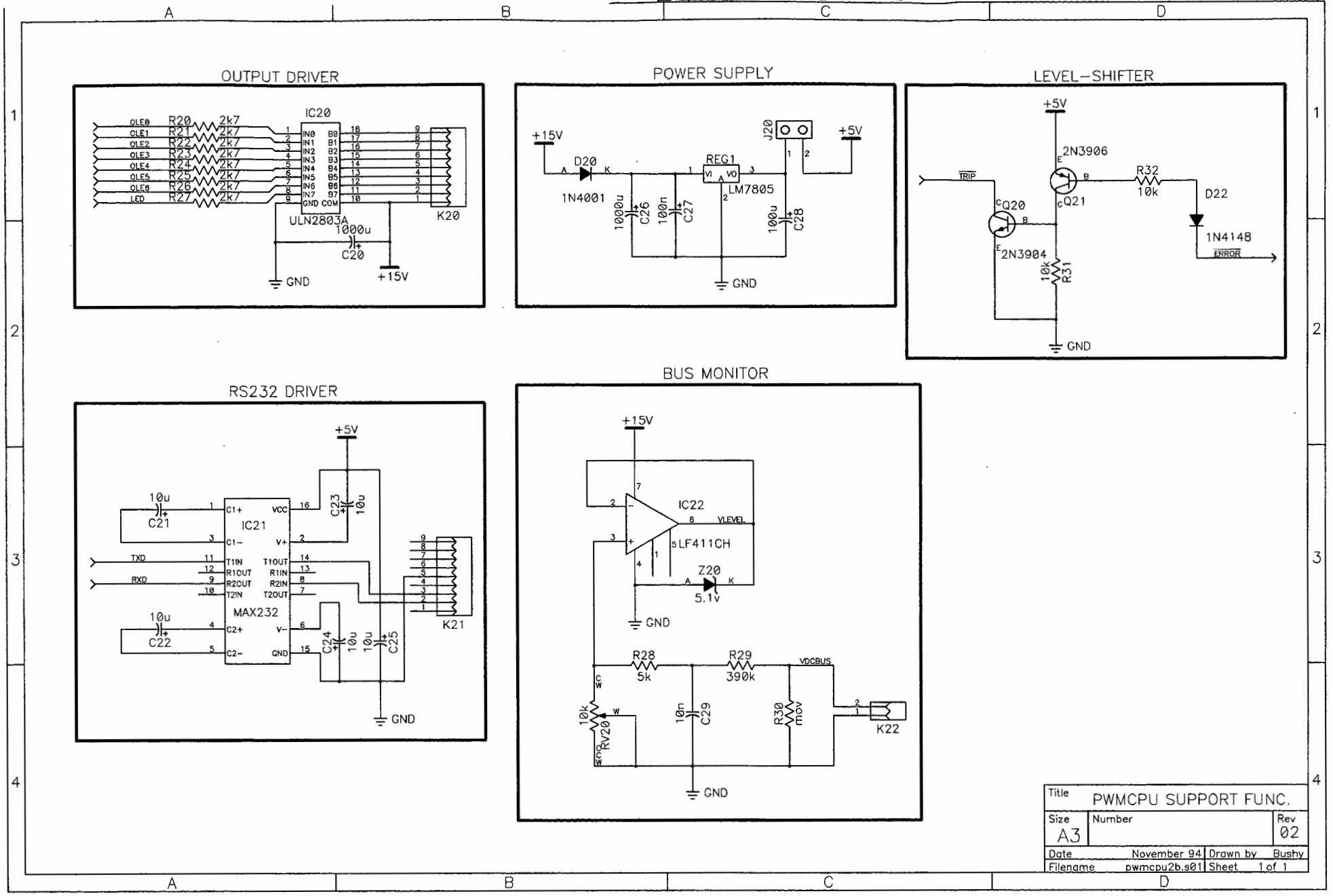
8254P
74HC573
27C256
22V10
16R8
IDC2X17M
IDC2X10M
16MHz
2N2907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OLE1
OLE2
OLE3
OLE4
OLE5
OLE6
LED
R20
R21
R22
R23
R24
R25
R26
R27
2k7
ULN2803A
K20
1000u
C20
GND
+15V
POWER SUPPLY
+15V
D20
1N4001
REG1
LM7805
J20
+5V
1000u
C26
100n
C27
100u
C28
GND
LEVEL-SHIFTER
+5V
2N3906
TRIP
R32
10k
D22
1N4148
ERROR
Q20
2N3904
Q21
10k
R31
GND
RS232 DRIVER
+5V
10u
C21
IC21
C1+
C1-
VCC
V+
C23
10u
TXD
RXD
T1IN
R1OUT
R2OUT
T2IN
T1OUT
R1IN
R2IN
T2OUT
MAX232
10u
C22
C2+
C2-
V-
GND
C24
10u
10u
C25
K21
GND
BUS MONITOR
+15V
IC22
VLEVEL
LF411CH
Z20
5.1v
GND
R28
5k
R29
390k
VDCBUS
10k
RV20
10n
C29
R30
mov
K22
GND
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Date
November 94
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Sheet
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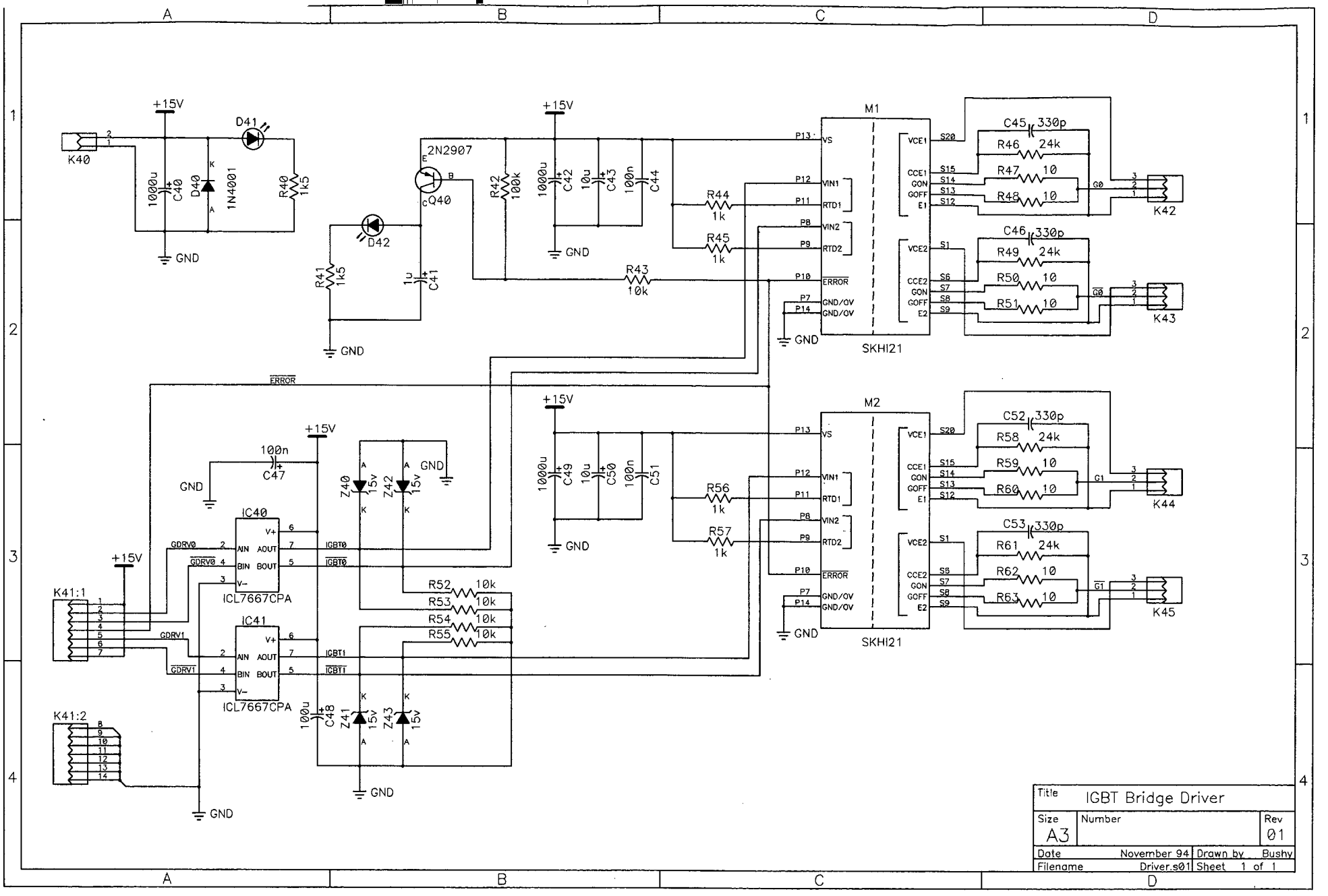
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Q40
R42 100k
1000u C42
10u C43
100n C44
D42
R41 1k5
1u C41
R44 1k
R45 1k
R43 10k
M1
P13 VS
P12 VIN1
P11 RTD1
P8 VIN2
P9 RTD2
P10 ERROR
P7 GND/OV
P14 GND/OV
SKHI21
VCE1 S20
CCE1 S15
GON S14
GOFF S13
E1 S12
VCE2 S1
CCE2 S6
GON S7
GOFF S8
E2 S9
C45 330p
R46 24k
R47 10
R48 10
G0
K42
C46 330p
R49 24k
R50 10
R51 10
K43
ERROR
100n C47
IC40
IC41
ICL7667CPA
GDRV0
GDRV1
IGBT0
IGBT1
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Z42 15v
Z41 15v
Z43 15v
100u C48
K41:1
K41:2
R52 10k
R53 10k
R54 10k
R55 10k
M2
1000u C49
10u C50
100n C51
R56 1k
R57 1k
C52 330p
R58 24k
R59 10
R60 10
G1
K44
C53 330p
R61 24k
R62 10
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Rev 01
Date November 94
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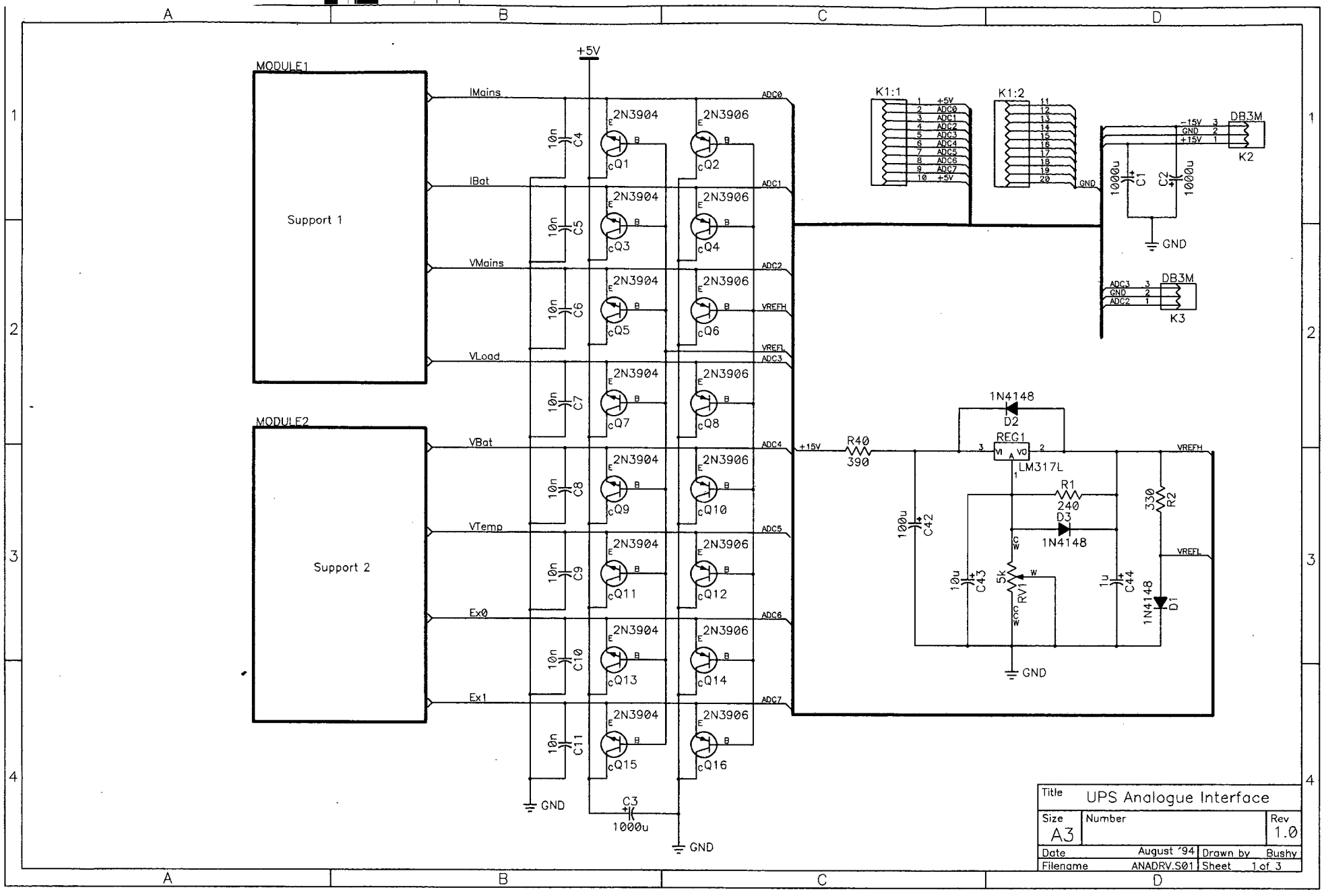
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Support 2
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VMains
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VBat
VTemp
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Ex1
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Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
C4
C5
C6
C7
C8
C9
C10
C11
10n
C3
1000u
GND
ADC0
ADC1
ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
VREFH
VREFL
K1:1
K1:2
DB3M
K2
K3
C1
C2
1000u
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R40
390
1N4148
D2
REG1
LM317L
R1
240
D3
1N4148
330
R2
100u
C42
10u
C43
5k
RV1
1u
C44
D1
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Rev
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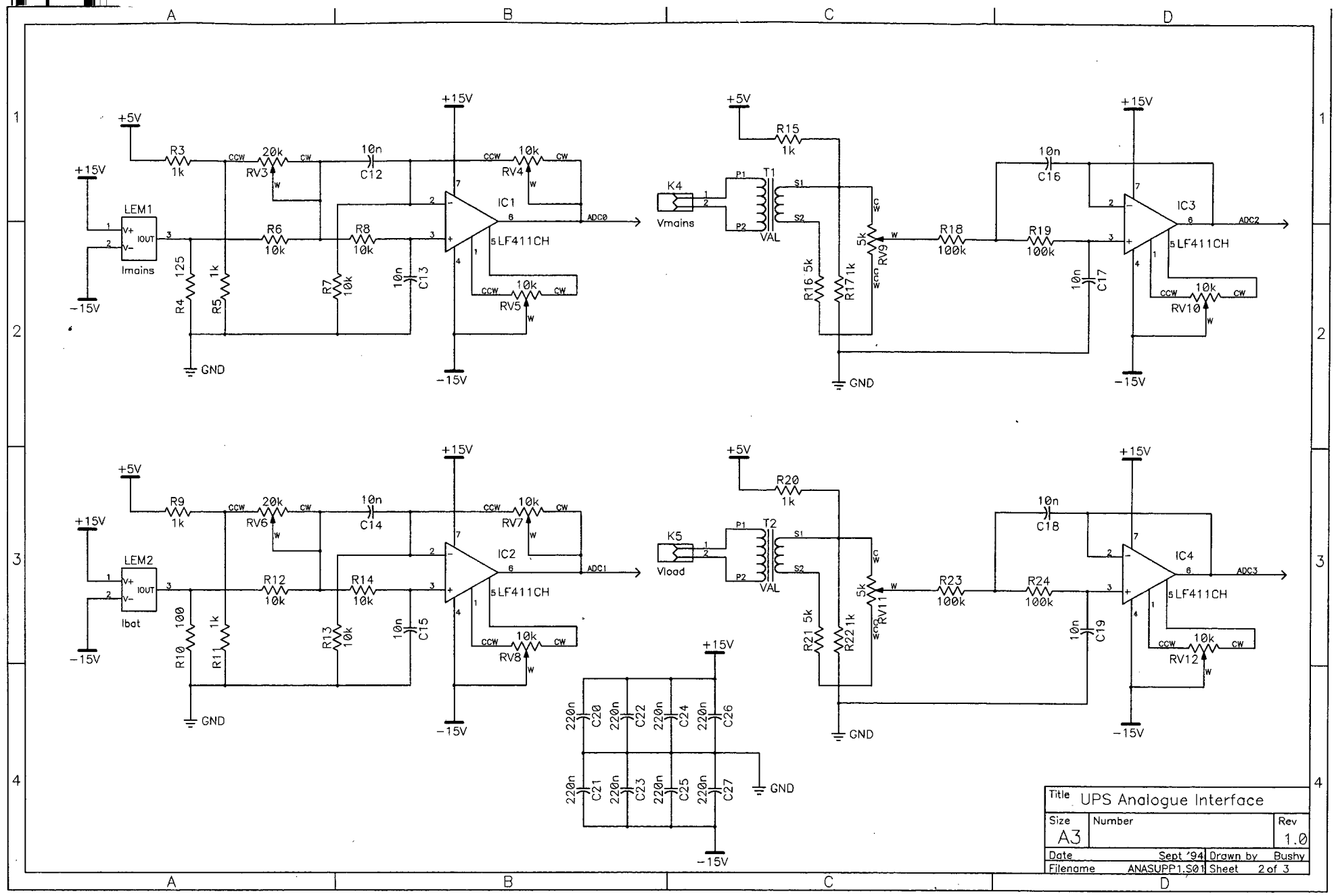
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B
C
D
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2
3
4
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+5V
-15V
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LEM1
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LEM2
Ibat
R3 1k
RV3 20k
C12 10n
RV4 10k
IC1
LF411CH
ADC0
R6 10k
R8 10k
R7 10k
C13 10n
RV5 10k
R4 125
R5 1k
R9 1k
RV6 20k
C14 10n
RV7 10k
IC2
ADC1
R12 10k
R14 10k
R13 10k
C15 10n
RV8 10k
R10 100
R11 1k
K4
Vmains
K5
Vload
T1
T2
P1
P2
S1
S2
VAL
R15 1k
R16 5k
R17 1k
RV9 5k
C16 10n
IC3
ADC2
R18 100k
R19 100k
C17 10n
RV10 10k
R20 1k
R21 5k
R22 1k
RV11 5k
C18 10n
IC4
ADC3
R23 100k
R24 100k
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C22 220n
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C24 220n
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Rev 1.0
Date Sept '94
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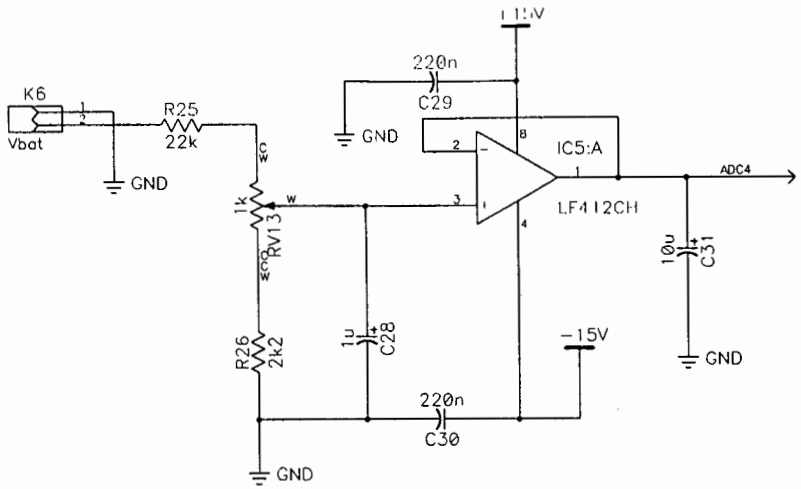
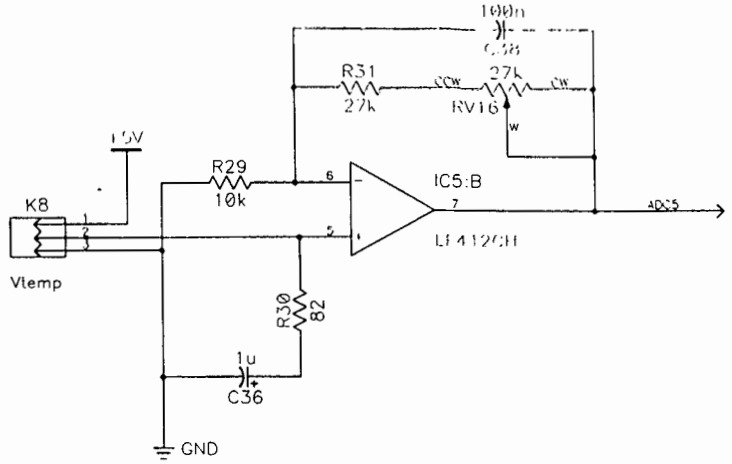
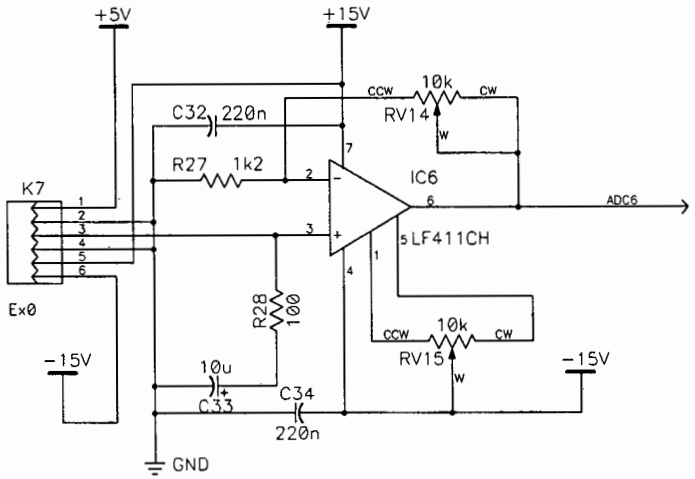
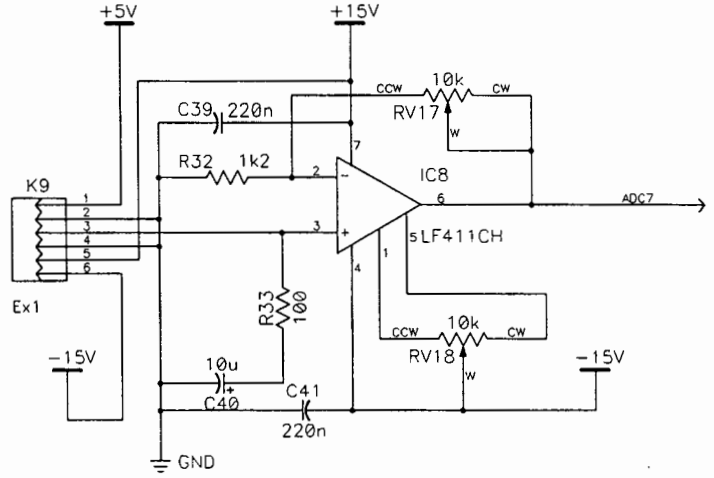
Sheet 2 of 3

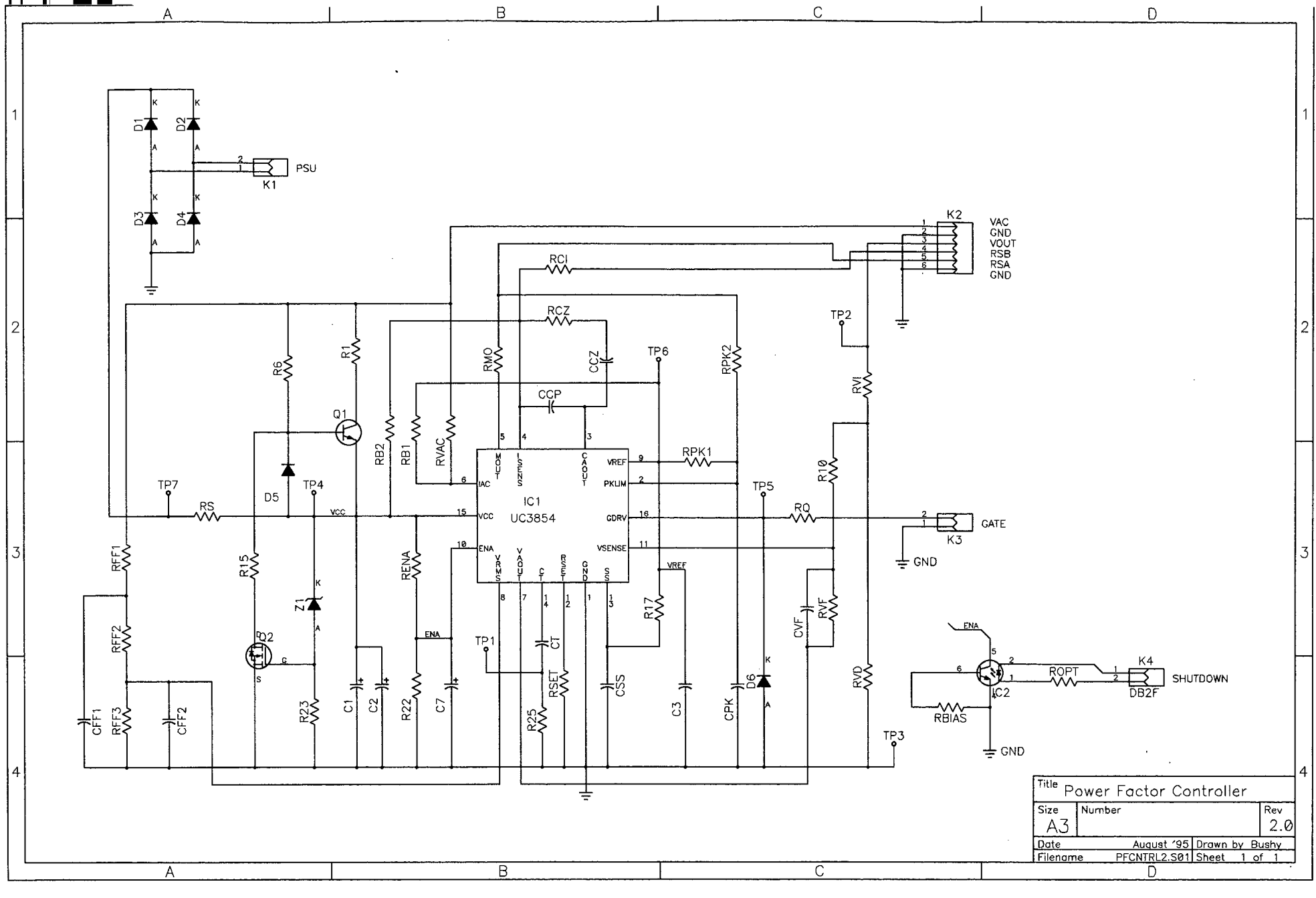


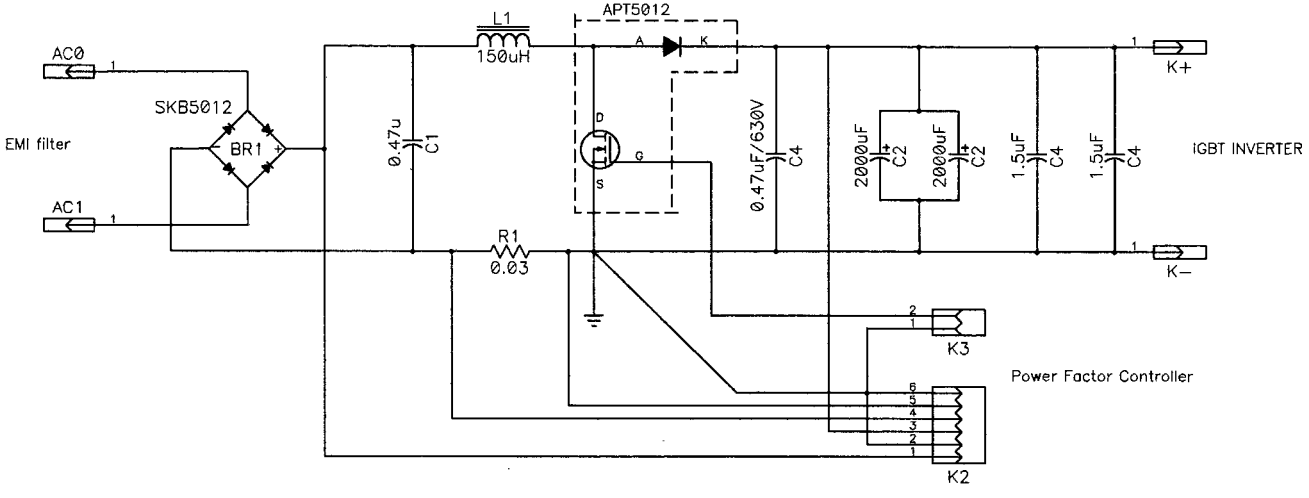




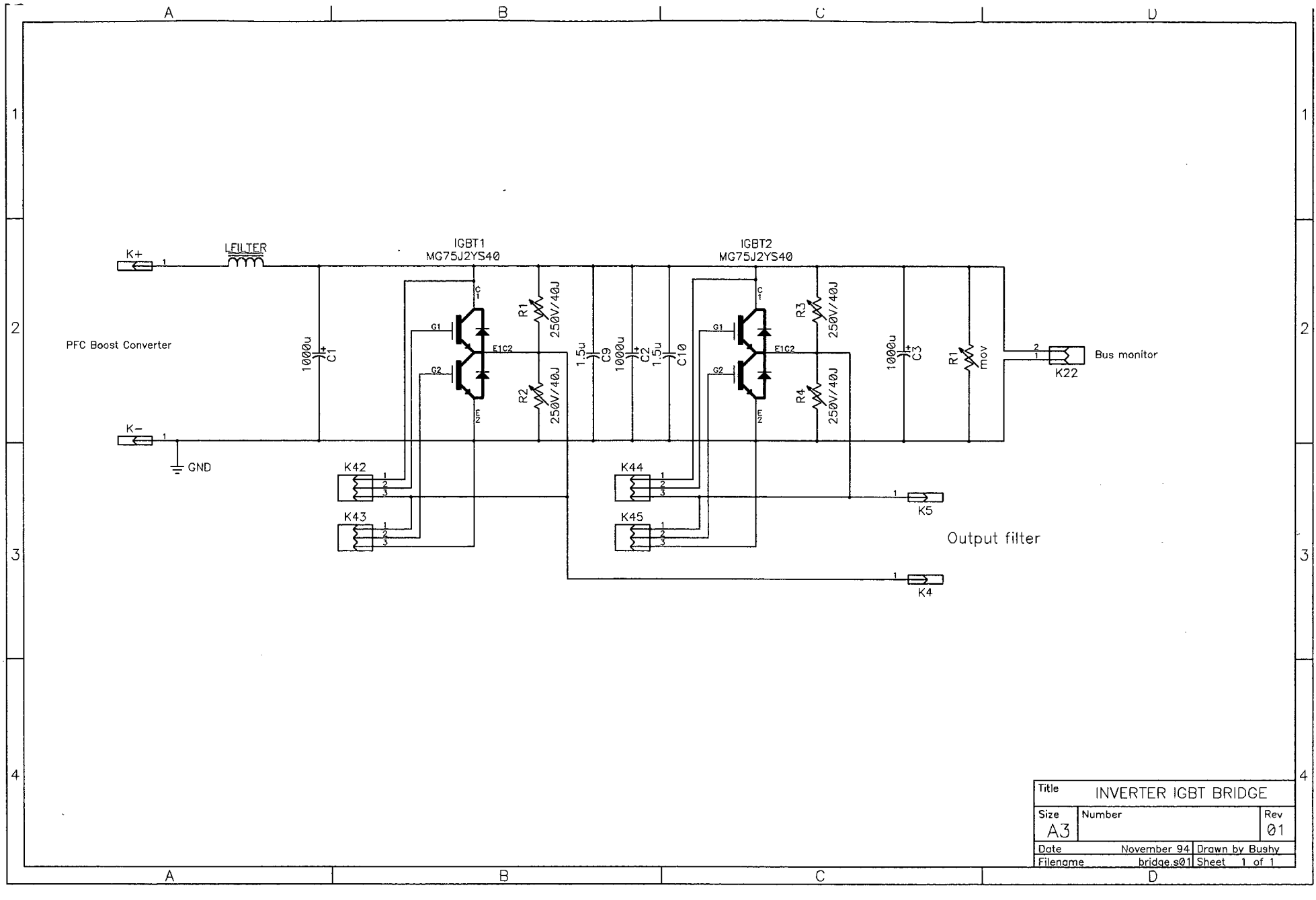


Title	UPS Analogue Interface		
Size A3	Number		Rev 1.0
Date	Sept '94	Drawn by	Bushy
Filename	ANASUPP2.S01	Sheet	3 of 3


D1
D2
D3
D4
PSU
K1
K2
VAC
GND
VOUT
RSB
RSA
GND
RCI
RCZ
CCZ
CCP
RMO
RPK2
RPK1
RVI
R10
RO
R1
R6
RB1
RB2
RVAC
Q1
D5
TP2
TP4
TP5
TP6
TP7
RS
IC1
UC3854
VREF
PKLIM
GDRV
VSENSE
VCC
ENA
IAC
GATE
K3
GND
RFF1
RFF2
RFF3
CFF1
CFF2
R15
Z1
D2
R23
C1
C2
RENA
R22
C7
TP1
CT
RSET
R25
CSS
C3
R17
CVF
RVF
CPK
D6
RVD
TP3
K4
ROPT
SHUTDOWN
DB2F
RBIAS
C2
Title
Power Factor Controller
Size
A3
Number
Rev
2.0
Date
August '95
Drawn by Bushy
Filename
PFCNTRL2.S01
Sheet 1 of 1



Title	PFC BOOST CONVERTER		
Size A3	Number		Rev 1.0
Date	Sept '94	Drawn by	Bushy
Filename	BOOST.S01	Sheet	1 of 1


K+
LFILTER
IGBT1
MG75J2YS40
IGBT2
MG75J2YS40
PFC Boost Converter
1000u
C1
R1
250V/40J
R2
250V/40J
1.5u
C9
1000u
C2
1.5u
C10
R3
250V/40J
R4
250V/40J
1000u
C3
R1
mov
Bus monitor
K22
K-
GND
K42
K43
K44
K45
K5
K4
Output filter
Title
INVERTER IGBT BRIDGE
Size
A3
Number
Rev
01
Date
November 94
Drawn by Bushy
Filename
bridge.s01
Sheet 1 of 1

Appendix F : Software listing

The following "C" listings are included:

- UPSKern.h - Kernel header definitions
- UPSKern.c - Kernel code

```
/*              Uninterruptible Power Supply KERNEL Controller

    Filename:   UPSKern.h
    Author   :  CJM
    Date     :  2/09/94
    Revision:   1.0
    Compiler:   Franklin C51 V8.63 / KeilC V5.10
    Platform:   A.E.C

    Purpose :   Kernel code for the uninterruptible power supply

    Notes   :

    Resources   : 32kB + Timer 0,1,2 + CT + ADC + watchdog
    Known BUGS  : None

 ******************************************************************************/
#ifndef __UPSKERN_H
#define __UPSKERN_H

// OPERATING PARAMETERS
#define DEF_OUTPUT_FREQUENCY        50  // Hz
#define DEF_REGULATION_SETPOINT     220 // Vrms
#define PMAX                        5000 // Watts
#define DEF_MIN_DCBUS               250 // Vrms-10%
#define DEF_MAX_DCBUS               395 // Vrms+10%
#define DEF_DCBUS_STARTUP           320 // Vdc
#define DEF_RIPPLE_PERIOD           50  // No. of 50Hz cycles to average over
#define DEF_RIPPLE_BAND             10  // Vdc Tolerable DC bus ripple voltage
#define DEF_BATTERY_LOW             120 // Vdc
#define DEF_BATTERY_FLOAT           165 // Vdc
#define DEF_BATTERY_BOOST           172 // Vdc
#define DEF_SINK_TEMP_TRIP          80  // degC
#define DEF_BAT_TEMP_TRIP           40  // degC
#define DEF_FAN_ON_TEMP             35  // degC
#define DEF_FAN_OFF_TEMP            25  // degC
#define DEF_CONFIG                  0x75

// INTERNAL SETPOINTS (all assume 18MHz clock)
#define DEF_PWMISR_CYCLES           341 // =276us of ISR time allocated
#define DEF_T2_RELOAD               (0xFFFF-DEF_PWMISR_CYCLES)
#define DEF_PHASE_INCREMENT         (DEF_OUTPUT_FREQUENCY*1491308/100000)

#define CHARGEUP_TIME               100 // *43ms=4.3 seconds
#define DISCHARGE_TIME              255 // *43ms=10.965 seconds
#define WAIT_4_RELAY                3   // *43ms=129ms
#define WAIT_4_PFC                  100 // *43ms=4.3 seconds
#define WAIT_4_INVERTER             100 // Wait for output voltage stabilise
#define INVERTER_VDROP              10  // Voltage drop across IGBTs + filter

#define ADCNOISE_LEVEL              4   // Uncertainity in ADC value
#define TEMPTOL                     10  // Temperature hystersis band
#define MAX_MA_ADJSTEP              5   // Maximum output voltage adj. step
#define MAX_CHARGER_DUTY            200 // Charger duty cycle
#define MAX_BULK_CURRENT            5   // Maximum charger current
#define MAX_BOOST_CURRENT           1   // Boost to standby transfer current
#define WATCHDOG_INTERVAL           0   // Watchdog reset time interval

// ALARM / MESSAGENO's
#define BatteryFault                1
#define ChargerFault                2
#define PFCTemp                     3
#define INVTemp                     4
#define IGBTFault                   5
#define SensorFault                 6
#define MAINS_FAILURE               7
#define SHUTDOWN                    8

#define FRONT_END_FAILURE           10
```

```
#define PFC_FAILURE                 11

#define TRIP                        0
#define RUN                         1
#define TEST                        2
#define UNDEFINED                   245
#define NO_CAN_DO                   254
#define NOCMD                       255
#define NOMSG                       255
#define NOALARM                     255
#define NORMAL                      0

// Message no's
#define CHARGING_BUS                20
#define DISCHARGING_BUS             21

#define BLEEDER_ON          {P5&=0xFE;P1&=0x7F;}    // D10
#define BLEEDER_OFF         {P5|=0x01;P1|=0x80;}
#define FAN_ON              {P5|=0x02;}
#define FAN_OFF             {P5&=0xFD;}
#define BYPASS_ON           {P5|=0x04;}
#define BYPASS_OFF          {P5&=0xFB;}
#define BATPACK_ON          {P5|=0x08;}
#define BATPACK_OFF         {P5&=0xF7;}
#define IN_RUSH_LIMIT_OFF   {P5|=0x30;P1|=0x20;}    // D8
#define IN_RUSH_LIMIT_ON    {P5&=0xCF;P1&=0xDF;}
#define PFC_ON              {P5&=0xBF;P1&=0xBF;}    // D9
#define PFC_OFF             {P5|=0x40;P1|=0x40;}
#define LED_ON              {P6&=0xFE;}
#define LED_OFF             {P6|=0x01;}

#define BLEEDER_ENABLED     (0==(P5&0x01))
#define FAN_ENABLED         (P5&0x02)
#define BYPASS_ENABLED      (P5&0x04)
#define BATPACK_ENABLED     (P5&0x08)
#define IN_RUSH_LIMIT_ENABLED (0==(P5&0x30))
#define PFC_ENABLED         (0==(P5&0x40))

// CHARGER STATES
#define BulkCharge          0           //
#define BoostCharge         1           //
#define FloatCharge         2           //

// GLOBAL DATA
typedef struct{
   uint STATUS;                         // System status
   uint MESSAGENO;                      // Associated status message
   uint ALARM;
   uint COMMAND;                        // Command to process

   uint IBAT;
   uint IOUT;
   uint VLINE;                          // AC input voltage level
   uint VOUT;                           // Output voltage level
   uint VBAT;
   uint VINV_TEMP;                      // Inverter heatsink temperature
   uint VAMBIENT_TEMP;                  // Ambient temperature
   uint VDC_BUS;                        // DC bus voltage

   uint REGULATION_SETPOINT;            // Inverter output voltage (peak)
   uint VCNTRL_P,VCNTRL_I,VCNTRL_D;     // Voltage controller parameters

   uint MIN_DCBUS;                      // Level to transfer to battery pack
   uint MAX_DCBUS;                      // Level to shutdown PFC
   uint DCBUS_STARTUP;                  // Voltage at which to disable bypass
   uint RIPPLE_PERIOD;                  // No. of cycles to average over
   uint RIPPLE_IDX;                     // Current ripple cycle
   uint RIPPLE;                         // Calculated DC bus ripple voltage
   uint RIPPLE_SHIFT;                   // Shift to minimise DC bus ripple
```

```
    uint RIPPLE_VMIN,RIPPLE_VMAX;       // Min/max bus voltage in current cycle

    uint PHASE_ACCUMULATOR;             // PWM table index
    uint PHASE_INCREMENT;               // Sets the output frequency
    uint CYCLE_COUNTER;                 // No. of output cycles completed

    uint BATTERY_LOW;                   // Level for UPS shutdown
    uint BATTERY_FLOAT;                 // Charger float voltage level
    uint BATTERY_BOOST;                 // Charger boost voltage level
    uint CHARGER_PWM;                   // Current pulse duty cycle
    uint CHARGER_STATE;                 // Boosting, floating etc.
    uint ADC_CHANNEL;                   // Current signal being digitized
    uint PWM_MA;                        // Modulation amplitude
    uint SINK_TEMP_TRIP;                // Heatsink over-temperature triplevel
    uint BATTERY_TEMP_TRIP;             //
    uchar IOLATCH;                      // IO latch state
    uchar CONFIG;                       // Software configuration bits
    uint MODE;

    uint ScaleFactor[16];               // 0,1-VLINE; 2,3-VBAT etc
} sUPS;

// Modbus - AEC driver interface
#define DEVICE_ADDRESS              16  //Modbus slave device address
#define DSTRUCT_SIZE                (sizeof(sUPS)>>1)

#ifdef __UPSKERN_C
    // Sine wave table used to generate the regular-sampled unipolar PWM
    code uchar SINETABLE[256]={
        128,131,134,137,140,143,146,149,152,156,159,162,165,168,171,174,176,
        179,182,185,188,191,193,196,199,201,204,206,209,211,213,216,218,220,
        222,224,226,228,230,232,234,235,237,239,240,242,243,244,246,247,248,
        249,250,251,251,252,253,253,254,254,254,255,255,255,255,255,255,255,
        254,254,253,253,252,252,251,250,249,248,247,246,245,244,242,241,239,
        238,236,235,233,231,229,4Q2,225,223,221,219,217,215,212,210,207,205,
        202,200,197,195,192,189,186,184,181,178,175,172,169,166,163,160,157,
        154,151,148,145,142,138,135,132,129,126,123,120,117,113,110,107,104,
        101,98,95,92,89,86,83,80,77,74,71,69,66,63,60,58,55,
        53,50,48,45,43,40,38,36,34,32,30,28,26,24,22,20,19,
        17,16,14,13,11,10,9,8,7,6,5,4,3,3,2,2,1,
        1,0,0,0,0,0,0,0,1,1,1,2,2,3,4,4,5,
        6,7,8,9,11,12,13,15,16,18,20,21,23,25,27,29,31,
        33,35,37,39,42,44,46,49,51,54,56,59,62,64,67,70,73,
        76,79,81,84,87,90,93,96,99,103,106,109,112,115,118,121,124,127};

    #define ADC_SEQSIZE 24
    code uchar ADC_SAMPLE_SEQ[ADC_SEQSIZE]={    0,1,7,  0,3,7,
                                                0,2,7,  0,4,7,
                                                0,3,7,  0,5,7,
                                                0,3,7,  0,6,7   };

    bdata uchar CONFIG;                 // Global code block enable
    sbit USES_PFC=CONFIG^0;
    sbit USES_VOLTAGE_REGULATOR=CONFIG^1;
    sbit USES_RIPPLE_REGULATOR=CONFIG^2;
    sbit USES_BATTERY_CHARGER=CONFIG^3;
    sbit USES_PLL=CONFIG^4;
    sbit USES_ADC=CONFIG^5;
    sbit USES_SOFT_STARTSTOP=CONFIG^6;
    sbit USES_CURRENT_REGULATOR=CONFIG^7;

    bit PowerFailure;
    bit NewCycle;                       // Phase accumulator roll
    data uchar SampleIdx;               // ADC sequencer index
    data uchar Tick;                    // Timer for contactors

    data uchar RIPPLE_SHIFT,RIPPLE_IDX; // Shift to minimise DC bus ripple
    data uint PHASE_ACCUMULATOR;        // PWM table index
    data uint PHASE_INCREMENT;          // Sets the output frequency
```

```
    data uint CYCLE_COUNTER;                //
    data uchar ADC_CHANNEL;                 // Current ADC channel
    data uchar RawADC[8];

    data uchar PWM_MA;                      // Modulation amplitude
    data uchar PowerUpState;                // State-machine index
    xdata sUPS SYS;                         // System variables
    xdata uchar PWMLookup[128][128];        // Quick scale lookup

    void CommandProcessor();
    void InitSystem();
    void PowerUp();
    void PowerDown();
    void RestartInverter();
    void UpdateIC();
#else
    extern code uchar SINETABLE[256];
    extern data uchar RIPPLE_SHIFT,RIPPLE_IDX;
    extern data uint PHASE_ACCUMULATOR;
    extern data uint PHASE_INCREMENT;
    extern data uint CYCLE_COUNTER;
    extern data uchar ADC_CHANNEL;
    extern data uchar RawADC[8];
    extern data uchar PWM_MA;
    extern xdata sUPS SYS;
#endif

#endif
//-------------------------------------------------------------------------TheEnd
```

```
/*              Uninterruptible Power Supply KERNEL Controller

    Filename:   UPSKern.h
    Author  :   CJM
    Date    :   2/09/94
    Revision:   1.0
    Compiler:   Franklin C51 V8.63 / KeilC V5.10
    Platform:   Onthou A.E.C verwyderings permit nommer

    Purpose :   Kernel code for the uninterruptible power supply

    Notes   :

    Resources   : 32kB + Timer 0,1,2 + CT + ADC + watchdog
    Known BUGS  : None

 ***************************** REVISION HISTORY ******************************
 Date: 2/10/95
 Mod: Blew MOSFET - included PFC power-up/down

 Date: 7/4/96
 Mod: IGBT+MOSFET overheat - replaced sink.

 Date: 22/10/97
 Mod: Blew 552 - replaced with 517
 ***************************** COMPILER SETUP ******************************/
#pragma NOMOD517 OE CD DB SB OT(6,SPEED) LARGE
#define __UPSKERN_C
#define VERSION    1
#define REVISION   0
#define DEBUG
//#define USES_WATCHDOG
/********************************** TAG ***********************************/
static code char STAG[]="Supply Friendly Uninterruptible Power Supply V2.0\n";
static code char HTAG[]="PWMCPU2a-c.sch, DRVCARD.pcb\n";
static code char Author[]="CJM";
static code char Source[]=__FILE__;
static code char Date[]=__DATE__;
static code char Time[]=__TIME__;
/*****************************************************************************/
#include<reg517a.h>                     // Processor definitions
#include<80C517.h>                      // Faster printf, memcpy etc.
#include<absacc.h>                      // Allow DMA
#include<std.h>                         // All standard functions/prototypes
#include<hexload.h>                     // HEXLoad version info support

#include"UPSkern.h"
#include"modbus.h"                      // Modicon Protocol Support
#include"control.h"

/********************************* M A I N ********************************/
void main()
{
   XWORD[AppPtr]=STAG;                  // Press 'V' to show software info
   XWORD[HardWPtr]=HTAG;                // Press 'H' to show hardware info

   InitCOM(COM1,b19200);
   InitSystem();

   EAL=1;
   while(1){
       switch((uchar)SYS.STATUS){
           case TRIP: break;
           case RUN:
               if(USES_ADC){
                   if(USES_VOLTAGE_REGULATOR)
                       VoltageRegulator();
                   else
                       SYS.PWM_MA=PWM_MA=CalcDCBusMa();
```

```
            }else
                PWM_MA=SYS.PWM_MA;

            if(USES_RIPPLE_REGULATOR) RippleRegulator();
            if(USES_BATTERY_CHARGER) BatteryCharger();
            break;
        default:                        // Should never be executed...
            SYS.STATUS=TRIP;
            SYS.COMMAND=NOCMD;
            SYS.MESSAGENO=NOMSG;
            SYS.MODE=TEST;
    }
    #ifdef USES_WATCHDOG
        RESET_WATCHDOG
    #endif
    CommandProcessor();
    UpdateIO();
}

/*-------------------------------------------------------------------------
  void PowerUp() - Brings the UPS on-line, enabling contactors, PFC,
  inverter as required.
 -------------------------------------------------------------------------*/
void PowerUp()
{
  if(USES_ADC){
    switch(PowerUpState){
        case 0:
            BLEEDER_OFF;
            IN_RUSH_LIMIT_ON;
            ++PowerUpState;
            break;
        case 1:
            if(SYS.VDC_BUS>SYS.MIN_DCBUS){
                IN_RUSH_LIMIT_OFF;
                Tick=WAIT_4_RELAY;
                ++PowerUpState;
            }
            break;
        case 2: if(0==Tick) ++PowerUpState; break;
        case 3: PFC_ON; FAN_ON; ++PowerUpState; break;
        case 4: if(SYS.VDC_BUS>SYS.DCBUS_STARTUP) ++PowerUpState; break;
        case 5:
            RestartInverter();
            Tick=WAIT_4_INVERTER;
            ++PowerUpState;
            break;
        case 6: if(0==Tick) ++PowerUpState; break;
        case 7:
            BYPASS_OFF;
            SYS.CYCLE_COUNTER=0;
            SYS.STATUS=RUN;
            break;
        default:
            PowerUpState=0;
    }
    SYS.IOLATCH=P5;
  }else{
    Tick=WAIT_4_RELAY;
    BLEEDER_OFF;
    IN_RUSH_LIMIT_ON;               // Should be on already but anyway...
    SYS.IOLATCH=P5;
    while(0!=Tick);

    Tick=CHARGEUP_TIME;
    SYS.MESSAGENO=CHARGING_BUS;
    while(0!=Tick);                 // DC bus slowly charges up

    Tick=WAIT_4_RELAY;
```

```
        IN_RUSH_LIMIT_OFF;
        SYS.IOLATCH=P5;
        while(0!=Tick);

        FAN_ON;                         // Cooling system on-line
        if(USES_PFC){
            PFC_ON;
            SYS.IOLATCH=P5;
            Tick=WAIT_4_PFC;
            while(0!=Tick);             // PFC boosts the DC bus voltage
        }

        RestartInverter();
        Tick=WAIT_4_INVERTER;
        SYS.IOLATCH=P5;
        while(0!=Tick);                 // Skip the filter transient period
        LED_ON;                         // Inverter up & running

        NewCycle=FALSE;
        while(!NewCycle);
        BYPASS_OFF;                     // Takeover load at next zero-crossing
        SYS.IOLATCH=P5;
        SYS.CYCLE_COUNTER=0;
        SYS.STATUS=RUN;
    }
}
/*-------------------------------------------------------------------------
    RestartInverter() - Sets up the compare timer and CCU for PWM generation
    on P4.0 and P4.1 (unipolar PWM)
 -------------------------------------------------------------------------*/
void RestartInverter()
{
    T2CON=0;                            // Stop timer 2

    // Compare timer setup - Compare mode 0, CM0 & CM1 enabled
    // NOTE: Writing to P4.0 or P4.1 has no effect if CMEN!=0
    CMSEL=0x00;                         // CMx assigned to Timer 2
    CMH0=0xFF;                          // Never changes (8-bit PWM for speed)
    CML0=0xFF;                          // Hold output low at power-up
    CMH1=0xFF;                          // Never changes (8-bit PWM for speed)
    CML1=0xFF;                          // Hold output low at power-up
    CMSEL=0x03;                         // CMx assigned to Comp. timer
    CMEN=0x03;                          // CMx enabled onto P4.0,P4.1

    CTCON&=0x70;                        // Flush previous setup (+T2PS1=0)
//  CTCON|=0x03;                        // Clk=Fosc/16 -> Fpwm=4394,53125Hz
    CTCON|=0x02;                        // Clk=Fosc/8 -> Fpwm=8789.0625Hz
    CTRELH=0xFF;                        // 0xFF??, only '?' must change
    CTRELL=0x00;                        // Kickstart->256 clocks till overflow

    SYS.PWM_MA=PWM_MA=CalcDCBusMa();
    SYS.PHASE_ACCUMULATOR=PHASE_ACCUMULATOR=0;
    SYS.RIPPLE_IDX=RIPPLE_IDX=0;
    SYS.RIPPLE_SHIFT=RIPPLE_SHIFT=0;
    SYS.CYCLE_COUNTER=0;

    // Power-up / RUN interrupt priority setup
    IP0&=0xC0;
    IP1&=0xC0;
    IP0|=0x05;
    IP1|=0x24;                          // EX1,T2,COM1,T0,T1
    IT1=1;                              // INT1 edge sensitive
    IE1=0;                              // Flush previous edge flag
    EX1=1;                              // Hardware fault detector enabled

    // Restart Timer 2
    CTCON&=0x7F;                        // Clear T2PS1 (clk prescaler bit)
    T2CON&=0x60;                        // Retain I3FR & I2FR bits
    T2CON|=0x11;                        // Auto-reload, Clk=Fosc/12, running
```

```
    TF2=0;
    ET2=1;                              // Enable PWM update
}
/*---------------------------------------------------------------------------
    void PowerDown() - Shutdown all systems and bypasses UPS
 ---------------------------------------------------------------------------*/
void PowerDown()
{
    IEN0|=0x88;                         // Insurance Timer 1 + global enabled

    Tick=WAIT_4_RELAY;
    PFC_OFF;
    SYS.IOLATCH=P5;
    while(0!=Tick);

    if(USES_PLL) PLL();                 // Phase-lock input-output waveforms

    NewCycle=FALSE;
    while(!NewCycle);
    BYPASS_ON;

    Tick=WAIT_4_RELAY;
    ET2=0;                              // Disable PWM update
    EX1=0;                              // Disable hardware fault detect
    CMEN&=0xFC;                         // Disable P4.0,P4.1 compare function
    P4&=0xFC;                           // PWM outputs = 0
    SYS.IOLATCH=P5;
    while(0!=Tick);

    Tick=WAIT_4_RELAY;
    BATPACK_OFF;
#ifndef DEBUG
    FAN_OFF;
#endif
    SYS.CHARGER_PWM=0;
    SYS.CHARGER_STATE=FloatCharge;
    IN_RUSH_LIMIT_ON;
    SYS.IOLATCH=P5;
    while(0!=Tick);

    Tick=DISCHARGE_TIME;
    BLEEDER_ON;                         // *** DPDT disconnects PFC from line
    SYS.IOLATCH=P5;
    SYS.MESSAGENO=DISCHARGING_BUS;
    while(0!=Tick);                     // Wait for DC BUS to discharge

    IP0&=0xC0;
    IP1&=0xC0;
    IP0|=0x09;
    IP1|=0x03;                          // COM1,T0,T1

    PowerUpState=0;
    SampleIdx=0;
    LED_OFF;
    SYS.IOLATCH=P5;
    SYS.STATUS=TRIP;                    // ->flush command
    SYS.CYCLE_COUNTER=CYCLE_COUNTER=0;
    SYS.PHASE_ACCUMULATOR=PHASE_ACCUMULATOR=0;
}
/*---------------------------------------------------------------------------
    void CommandProcessor() - Reacts to SYS.COMMAND by modifying SYS.STATUS,
    SYS.ALARM & SYS.MESSAGENO.
 ---------------------------------------------------------------------------*/
void CommandProcessor()
{
    if((NOCMD!=SYS.COMMAND)||(CMD_UPDATE)){

        if(NOALARM!=SYS.ALARM){
            SYS.COMMAND=NOCMD;
```

```
    }else{
        if(SYS.COMMAND==SYS.STATUS){
            SYS.COMMAND=NOCMD;
            SYS.MESSAGENO=NOMSG;
        }else{
            switch((uchar)SYS.COMMAND){
                case TRIP: PowerDown(); break;
                case RUN: PowerUp(); break;
                case TEST: SYS.MODE^=TEST; SYS.COMMAND=NOCMD; break;
                case NOCMD: break;
                default:            // *Unrecognised command*
                    SYS.ALARM=NO_CAN_DO;
                    SYS.MESSAGENO=SYS.COMMAND;
                    SYS.COMMAND=NOCMD;
            }
        }
    }
    CMD_UPDATE=FALSE;
}

/*-----------------------------------------------------------------------------
  void UpdateIO() - Enables disables contactors, indicators
-----------------------------------------------------------------------------*/
void UpdateIO()
{
  data uint Temp;

  ADC_CHANNEL&=0x07;                    // 0..7 valid channels

  if(USES_ADC){
      if(ET2&&IADC){
          Temp=(ADDATH * SYS.ScaleFactor[ADC_CHANNEL]) /
                  (uchar)SYS.ScaleFactor[ADC_CHANNEL|0x08];

          *(&SYS.IBAT+ADC_CHANNEL)=Temp;

          ADC_CHANNEL=ADC_SAMPLE_SEQ[SampleIdx];
          ++SampleIdx;
          if(SampleIdx==ADC_SEQSIZE) SampleIdx=0;

          ADCON0&=0xC0;                 // Allow a channel change
          ADCON0|=ADC_CHANNEL;          // Change channel
          IADC=0;                       // Flush isr flag
          ADDATL=0xFF;                  // Start the next conversion
      }
  else
      if(SYS.CONFIG&0x20){
          if(!BSY&&(0==IADC)){
              SampleIdx=0;
              SYS.ADC_CHANNEL=ADC_CHANNEL=ADC_SAMPLE_SEQ[0];
              ADCON0&=0xC0;
              ADCON0|=ADC_CHANNEL;

              /* CRITICAL */
              EAL=FALSE;
                  USES_ADC=TRUE;
                  ADDATL=0xFF;          // Kickstart
              EAL=TRUE;
          }
      }

  CONFIG=SYS.CONFIG;                    // Update all other USES_xxxx
  SYS.CYCLE_COUNTER=CYCLE_COUNTER;

  if((ET2&NewCycle)||!ET2){
      NewCycle=FALSE;
      if(TEST==SYS.MODE){
          if(!USES_RIPPLE_REGULATOR) RIPPLE_SHIFT=SYS.RIPPLE_SHIFT;
```

```
        PHASE_INCREMENT=SYS.PHASE_INCREMENT;// Modify the output frequency

        // Smoke prevention checks
        if(0==(SYS.IOLATCH&0x01)){          // Bleeder ON
            SYS.IOLATCH|=0x40;              // -> PFC off
            P1&=0x7F;                       // -> Turn D10 LED on
        }else
            P1|=0x80;

        if(USES_PFC){
            if(0==(SYS.IOLATCH&0x40)){      // PFC ON
                SYS.IOLATCH|=0x31;          // -> Inrush + bleeder off
                P1|=0xA0;                   // -> Turn D8, D10 LED off
                P1&=0xBF;                   // -> Turn pfc D9 LED on
            }else
                P1|=0x40;
        }else{
            SYS.IOLATCH|=0x40;
            P1|=0x40;
        }

        if(0==(SYS.IOLATCH&0x10)){          // Inrush ON
            SYS.IOLATCH&=0xCF;
            if(ET2){
                SYS.IOLATCH|=0x30;          // Inverter active->inrush off
                P1|=0x20;                   // Turn D8, inrush LED off
            }else
                P1&=0xDF;
        }else{
            SYS.IOLATCH|=0x30;
            P1|=0x20;
        }
        P5=SYS.IOLATCH;
    }else{
        if(TRIP==SYS.STATUS){
            BLEEDER_ON;
            BYPASS_ON;
            IN_RUSH_LIMIT_ON;
            PFC_OFF;
            LED_OFF;
            #ifdef DEBUG
                FAN_ON;
            #else
                if(SYS.VINV_TEMP<DEF_FAN_OFF_TEMP){
                    FAN_OFF;
                    SYS.IOLATCH&=0xFD;
                }
            #endif
        }
        SYS.PHASE_ACCUMULATOR=PHASE_ACCUMULATOR;
        SYS.ADC_CHANNEL=ADC_CHANNEL;
        SYS.IOLATCH=P5;
    }
    // Overheat over-ride
    if(SYS.VINV_TEMP>DEF_FAN_ON_TEMP){
        FAN_ON;
        SYS.IOLATCH|=0x02;
    }
  }
}
/*---------------------------------------------------------------------------
   void InitSystem() - Initializes controller variables & hardware
 ---------------------------------------------------------------------------*/
void InitSystem()
{
   uchar TabIdx,WaveIdx;
   uint PwmVal;

   BLEEDER_ON;                          // Dump the bus capacitor energy
```

```
#ifdef DEBUG
   FAN_ON;
#else
   FAN_OFF;
#endif
   BYPASS_ON;                          // Load supplied by line not UPS
   BATPACK_OFF;
   IN_RUSH_LIMIT_ON;                   // Save the diode bridge & FRED
   PFC_OFF;
   LED_OFF;
   PowerUpState=0;
   P4&=0xFC;                           // Force IGBT PWM signals low

   SYS.STATUS=TRIP;
   SYS.MESSAGENO=TRIP;
   SYS.ALARM=NOALARM;
   SYS.COMMAND=NOCMD;

   SYS.IBAT=0;
   SYS.IOUT=0;
   SYS.VLINE=DEF_REGULATION_SETPOINT;
   SYS.VOUT=DEF_REGULATION_SETPOINT;
   SYS.VBAT=DEF_BATTERY_FLOAT;
   SYS.VINV_TEMP=0;
   SYS.VAMBIENT_TEMP=0;
   SYS.VDC_BUS=0;

   SYS.REGULATION_SETPOINT=DEF_REGULATION_SETPOINT;
   SYS.VCNTRL_P=CNTRLP;
   SYS.VCNTRL_I=CNTRLI;
   SYS.VCNTRL_D=CNTRLD;

   SYS.MIN_DCBUS=DEF_MIN_DCBUS;
   SYS.MAX_DCBUS=DEF_MAX_DCBUS;
   SYS.DCBUS_STARTUP=DEF_DCBUS_STARTUP;
   SYS.RIPPLE_PERIOD=DEF_RIPPLE_PERIOD;
   SYS.RIPPLE_IDX=RIPPLE_IDX=0;
   SYS.RIPPLE=0xFF;                    // Assume worst possible ripple
   SYS.RIPPLE_SHIFT=RIPPLE_SHIFT=0;
   SYS.RIPPLE_VMIN=0xFF;               // Kickstart min < vdc check
   SYS.RIPPLE_VMAX=0;                  //

   SYS.PHASE_ACCUMULATOR=PHASE_ACCUMULATOR=0;
   SYS.PHASE_INCREMENT=PHASE_INCREMENT=DEF_PHASE_INCREMENT;
   SYS.CYCLE_COUNTER=CYCLE_COUNTER=0;

   SYS.BATTERY_LOW=DEF_BATTERY_LOW;
   SYS.BATTERY_FLOAT=DEF_BATTERY_FLOAT;
   SYS.BATTERY_BOOST=DEF_BATTERY_BOOST;
   SYS.CHARGER_PWM=0;
   SYS.CHARGER_STATE=FloatCharge;      // Assume batteries are charged

   SYS.PWM_MA=PWM_MA=0;
   SYS.SINK_TEMP_TRIP=DEF_SINK_TEMP_TRIP;
   SYS.BATTERY_TEMP_TRIP=DEF_BAT_TEMP_TRIP;
   SYS.IOLATCH=P5;
   SYS.CONFIG=CONFIG=DEF_CONFIG;
   SYS.MODE=NORMAL;

   SYS.ScaleFactor[0]=10;              // IBat=.196078431373 R=100, 1000:1 LEM
   SYS.ScaleFactor[1]=10;              // Iout=.196078431373 R=100, 1000:1 LEM
   SYS.ScaleFactor[2]=50;              // VLine=.0980392156863
   SYS.ScaleFactor[3]=50;              // Vout=0.980392156863 5V=255=250Vrms
   SYS.ScaleFactor[4]=25;              // VBat=1.5625
   SYS.ScaleFactor[5]=25;              // VInvTemp
   SYS.ScaleFactor[6]=25;              // VAmbTemp=0.490196078431 LM35=10mV/C*4
   SYS.ScaleFactor[7]=26;              // Approx > VDCBus=1.5625 5V=255=400Vdc

   SYS.ScaleFactor[8]=51;              // IBat
```

```
    SYS.ScaleFactor[9]=51;              // Iout
    SYS.ScaleFactor[10]=51;             // VLine
    SYS.ScaleFactor[11]=51;             // Vout
    SYS.ScaleFactor[12]=16;             // VBat
    SYS.ScaleFactor[13]=51;             // VInvTemp
    SYS.ScaleFactor[14]=51;             // VAmbTemp
    SYS.ScaleFactor[15]=16;             // VDCBus

    DSTRUCT=&SYS;
    CMD_ADDRESS=(&SYS.COMMAND-&SYS.STATUS)+1;
    InitModBus();

    // Power-down / TRIP interrupt priority setup
    IP0&=0xC0;
    IP1&=0xC0;
    IP0|=0x09;
    IP1|=0x03;                          // COM1,T0,T1

    // Analog to digital converter setup
    ADCON1&=0xF0;                       // Flush channel selection
    ADCON1|=0x80;                       // ADCL=1 if Fosc>16MHz -> 12.4us/conv
    ADCON0&=0xC0;                       // Flush channel selection
    SampleIdx=0;
    if(USES_ADC){
        SYS.ADC_CHANNEL=ADC_CHANNEL=ADC_SAMPLE_SEQ[0];

        IADC=0;                         // Flush ISR flag
        ADCON0|=ADC_CHANNEL;            // Change channel
        ADDATL=0xFF;                    // Start the first conversion
    }

    // Timer 1 - clock tick
    TMOD&=0x0F;
    TMOD|=0x10;                         // 16-bit timer, runs continuously
    TCON&=0x3F;
    TR1=1;
    Tick=0;                             // Overflow counter (++ every 43.7ms)
    ET1=1;                              // Interrupt enabled

    // Timer 2 - PWM update
    CRCL=(uchar)DEF_T2_RELOAD;
    CRCH=DEF_T2_RELOAD>>8;              // Fixed time allocated to PWM isr
    CTCON&=0x7F;                        // Clear T2PS1 (clk prescaler bit)
    T2CON&=0x60;                        // Retain I3FR & I2FR bits
    T2CON|=0x11;                        // Auto-reload, Clk=Fosc/12, running
    ET2=0;                              // Disable interrupt

    // Generate PWM scaling table lookup
    for(TabIdx=0;TabIdx<0x80;++TabIdx){
        for(WaveIdx=0;WaveIdx<0x80;++WaveIdx){
            PwmVal=SINETABLE[WaveIdx]&0x7F;
            PwmVal*=(0x80+TabIdx);
            PWMLookup[TabIdx][WaveIdx]=PwmVal>>8;
        }
    }
    PowerFailure=FALSE;                 // Optimistic approach
}
/*****************************************************************************
 ********************** INTERRUPT SERVICE ROUTINES ***************************
 *****************************************************************************/
/*---------------------------------------------------------------------------
   HardwareFault() - Called by SKHI21 IGBT drivers on an overcurrent or
   other fault condition. Reset by turning both PWM inputs off.
 ---------------------------------------------------------------------------*/
void HardwareFault() interrupt INT_EX1 using 2 // P3.3
{
    ET2=0;                              // Disable PWM update
    CMEN=0;                             // Disable compare function
    P4&=0xFC;                           // PWM outputs = 0
```

```
    PFC_OFF;
    IN_RUSH_LIMIT_ON;
    BLEEDER_ON;
    FAN_OFF;
    BYPASS_ON;
    BATPACK_OFF;

    LED_OFF;

    SYS.STATUS=TRIP;
    SYS.COMMAND=NOCMD;
    SYS.ALARM=IGBTFault;                    // Over-current ?

#pragma MOD517
/*-------------------------------------------------------------------------
    PWMService() - Called by Timer 2 interrupt to update the PWM outputs.
 -------------------------------------------------------------------------*/
void PWMService( ) interrupt INT_T2 using 1
{
    data uchar WaveValue;
    data uint Temp,prevACC;

    prevACC=PHASE_ACCUMULATOR;
    PHASE_ACCUMULATOR+=PHASE_INCREMENT;

    if(USES_RIPPLE_REGULATOR)
        WaveValue=SINETABLE[((PHASE_ACCUMULATOR>>8)+RIPPLE_SHIFT)&0x7F];
    else
        WaveValue=SINETABLE[(PHASE_ACCUMULATOR>>8)&0x7F];

    Temp=(WaveValue & 0x7F)*PWM_MA;
    WaveValue=Temp>>8;
/*
#pragma ASM
    // Cut
#pragma ENDASM
*/
    if((PHASE_ACCUMULATOR>>8)&0x80)
        CML1=~(CML0=0x80-WaveValue);
    else
        CML1=~(CML0=WaveValue|0x80);

    /*-------------------------------------------------------------------------
        ADCService() - Converts each analog channel - in sync with the
        inverter PWM to reduce noise on readings.
     -------------------------------------------------------------------------*/
    if(IADC){
        RawADC[ADC_CHANNEL]=ADDATH;

        Temp=(ADDATH*SYS.ScaleFactor[ADC_CHANNEL]) /
                (uchar)SYS.ScaleFactor[ADC_CHANNEL|0x08];

        *(&SYS.IBAT+ADC_CHANNEL)+=Temp;
        *(&SYS.IBAT+ADC_CHANNEL)/=2;

        ADC_CHANNEL=ADC_SAMPLE_SEQ[SampleIdx++];
        if(SampleIdx==ADC_SEQSIZE) SampleIdx=0;
        IADC=0;
    }
    if(prevACC>PHASE_ACCUMULATOR){
        ++CYCLE_COUNTER;
        NewCycle=TRUE;
        SampleIdx=ADC_CHANNEL=0;     // Start new cycle channel @ VOUT
    }
    if(USES_ADC){
        ADCON0&=0xC0;                // Allow a channel change
        ADCON0|=ADC_CHANNEL;         // Change channel
        ADDATL=0xFF;                 // Start the next conversion
```

```
    TF2=0;
}
#pragma NOMOD51
/*------------------------------------------------------------------------
  ClockTick() - Decrements Tick every 43 milliseconds
 ------------------------------------------------------------------------*/
void ClockTick() interrupt INT_T1
{
  if(0!=Tick) --Tick;
}
/*------------------------------------------------------------------------TheEnd
```

Appendix G : Voltage adjustment by phase-shifting the inverter legs

The following MCS51 assembly code, called by the timer zero interrupt, was used to evaluate the phase-shifting voltage control method.

```
push PSW                ; Timer zero interrupt entry point
mov PSW,#Bank1
mov R0,A
mov R1,B
mov R2,DPL
mov R3,DPH

mov A,PhaseAccL         ; Update the frequency synthesis
                        ; accumulator
add A,PhaseIncL
mov PhaseAccL,A
mov A,PhaseAccH
addc A,PhaseIncH
mov PhaseAccH,A

mov DPTR,#MaTable       ; Get address of linearisation table
mov A,Ma
mov A,@A+DPTR
mov B,A                 ; Save table shift
inc DPH                 ; Move to the beta adjustment table
mov A,@A+DPTR
add A,PhaseAcc          ; Include beta correction to pointer
push ACC
mov A,@A+DPTR
mov PWM0,A              ; Update phase leg zero
pop ACC
add A,B
mov A,@A+DPTR
mov PWM1,A              ; Update phase leg one

mov DPH,R3              ; Restore all registers
mov DPL,R2
mov B,R1
mov A,R0
pop PSW
reti                    ; Return from interrupt, restoring program
                        ; counter
```

Appendix H : IEC555-2 Harmonic limits

The European and South African single phase electrical systems both distribute power at 220-250 volts. This implies the current is half that for an equivalent load operating on the 120 volt USA network, allowing smaller gauge wire and fuses. The disadvantage of this system is the increased sensitivity to circulating currents.

IEC 555 HARMONIC CURRENT LIMITS

Odd harmonics (n)	Class A limits (A)	Class D absolute (A)	Class D relative mA/W
3	2.30	1.08	3.6
5	1.14	0.60	2.0
7	0.77	0.45	1.5
9	0.44	0.30	1.0
11	0.33	0.18	0.6
13	0.21	0.15	0.51
15 to 39	0.15x(15/n)	0.18x(11/n)	0.6x(11/n)
Even harmonics			
2	1.08	.3	1
4	.43	.15	0.5
6	.3	-	-
8 to 40	0.23x(8/n)	-	-

Figure 1: International Electrotechnical Commission harmonic current limits

With the goal of minimising the circulating currents, the International Electrotechnical Committee (IEC) generated the IEC 555-2. This specification sets limits for currents at each harmonic frequency through the 40th harmonic. The IEC also divided equipment into four classes, each with its own set of harmonic current limits.

Power supply designers and users need only be concerned with two of the four classifications: Class A and D. Class D covers equipment with a "predefined" current waveform. Class A covers equipment that does not fall into one of the other categories. The odd harmonic limits for Class A equipment are twice as high as those for Class D. It is twice as hard to meet the Class D requirement as the Class A.

In Class A equipment the maximum third harmonic current is 2.3 amperes. In Class D it is limited to just 1.08 amperes. The third harmonic current drawn by a switch mode power supply without power factor correction is typically 82 percent of the fundamental current. This means an uncorrected switch mode power supply drawing more than 155 watts from the AC line will have a third harmonic current that exceeds the Class D limit. The same power supply could draw about 300 watts from the AC mains before it exceeded the third harmonic limit for Class A equipment. To qualify for Class A status, the dead angle of the current waveform must be less than 45 degrees. The rectifier must conduct for at least 315 degrees of each 360 degree input cycle. A 315 degree conduction angle yields a power factor between 0.85 and 0.90 - significantly higher than the 0.65 that is typical of an uncorrected switch-mode PSU.

Appendix I: The effect of a reactive load on the DC bus ripple regulator

In following analysis, the high-frequency switching effects of both the power factor corrector (PFC) and IGBT inverter are ignored.

Line frequency: $f := 50$

$\omega := 2 \cdot \pi \cdot f$

Load parameters: $Vrms := 1$

$Irms := 1$

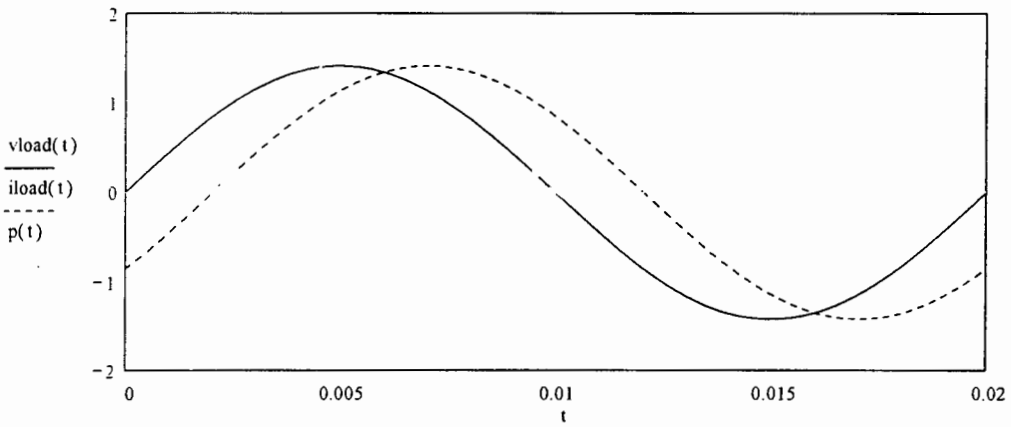
$pf := 0.8$

$vload(t) := \sqrt{2} \cdot Vrms \cdot \sin(\omega \cdot t)$

$iload(t) := \sqrt{2} \cdot Irms \cdot \sin(\omega \cdot t - \operatorname{acos}(pf))$

Instantaneous power: $p(t) := vload(t) \cdot iload(t)$

$t := 0, 0.0001 .. \frac{1}{f}$



Since power in a resistance is proportional to the square of the current, the instantaneous power is always positive. However, in reactive load, energy is exchanged between the source and load as illustrated above. At the start of the cycle p(t) is negative indicating a return of energy from the load. As the current passes through zero, energy is again absorbed by the load until the voltage goes negative. This exchange of energy limits the ability of the regulator to reduce the DC bus voltage ripple.

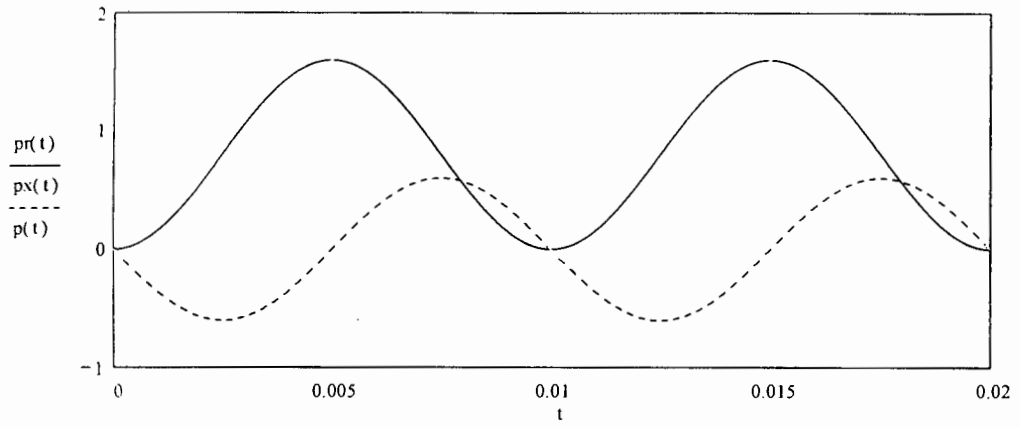
Re-arranging the instantaneous power, yields the real and reactive components:

$\phi := \operatorname{acos}(pf)$

$p(t) := 2 \cdot Vrms \cdot Irms \cdot \left[\sin(\omega \cdot t)^2 \cdot \cos(\phi) - \sin(\omega \cdot t) \cdot \cos(\omega \cdot t) \cdot \sin(\phi) \right]$

Real power: $pr(t) := 2 \cdot Vrms \cdot Irms \cdot \sin(\omega \cdot t)^2 \cdot \cos(\phi)$

Reactive power: $px(t) := -Vrms \cdot Irms \cdot \sin(2 \cdot \omega \cdot t) \cdot \sin(\phi)$



The PFC is a unidirectional source by virtue of the boost diode. Therefore the reactive load power must be supplied by the DC bus capacitance. This exchange of energy results in a DC bus voltage ripple.

PFC regulation setpoint: $Vav := 1$

Ripple voltage: $Vr := 1$

DC bus capacitance: $C := 1$

Calculate the change in energy

$$Emin := \frac{1}{2} \cdot C \cdot (Vav - Vr)^2$$

$$Emax := \frac{1}{2} \cdot C \cdot (Vav + Vr)^2$$

$$Echg := \frac{1}{2} \cdot C \cdot \left[(Vav + Vr)^2 - (Vav - Vr)^2 \right]$$

Simplifying yields $Echg := 2 \cdot C \cdot Vav \cdot Vr$

Equating reactive load power and bus capacitance ripple energy...

$$2 \cdot C \cdot Vav \cdot Vr = \frac{4}{T} \cdot \int_0^{\frac{T}{4}} |px(t)| \, dt$$

Since $\omega = 2 * \pi * f$ $\quad T = \frac{2 \cdot \pi}{\omega}$

After simplifying yields the following expression for the DC bus ripple magnitude

$$Vr := \frac{Vrms \cdot Irms \cdot \sin(\phi)}{\pi \cdot C \cdot Vav} \qquad Vr = 0.191$$

The above expression is the minimum ripple that can be expected on the DC bus for a reactive load. It assumes the delivery of current by the PFC and the extraction of current by the load are in phase i.e capacitor current Ic=0.

If this is not the case, an addition ripple due to the difference current must also be included.

PFC current: $Ipfc := \sqrt{2} \cdot Irms$

$$ipfc(t) := Ipfc \cdot \sin(\omega \cdot t)$$

The ripple regulator reduces the DC ripple by shifting the inverter phase voltage relative to the incoming voltage to synchronise the currents.

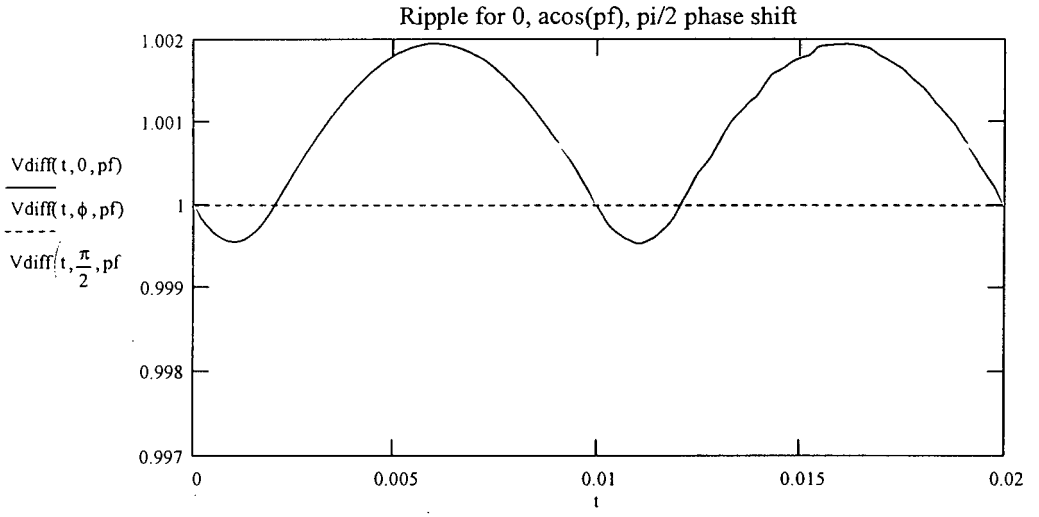
$$iload(t, \alpha, pf) := \sqrt{2} \cdot Irms \cdot \sin(\omega \cdot t - \operatorname{acos}(pf) + \alpha)$$

The difference current is...

$$idiff(t, \alpha, pf) := ipfc(t) - iload(t, \alpha, pf)$$

Integrating yields the difference voltage

$$Vdiff(t, \alpha, pf) := \frac{1}{C} \cdot \int_0^t idiff(t, \alpha, pf)\, dt + Vav$$



Appendix J: Power factor corrector MOSFET and diode loss calculation

Operating parameters:

Boost inductance: $L := 500 \cdot 10^{-6}$

Line voltage (peak): $Vm := 255$ Output voltage: $Vo := 380$

Line current (peak): $Ip := 36$

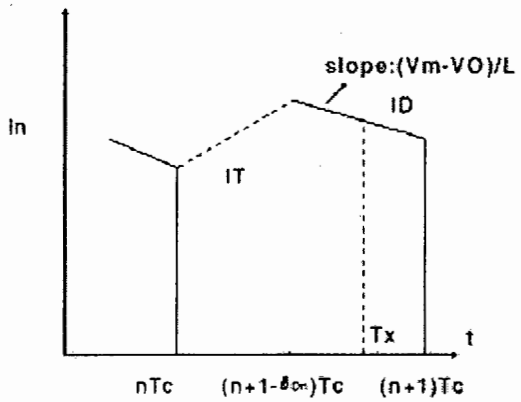
Line frequency: $F := 50$ $T := \frac{1}{F}$

Switching frequency: $Fc := 100 \cdot 10^{3}$

$Tc := \frac{1}{Fc}$

Diode power losses

The diode power loss is the sum of the conduction, reverse and switching losses.



Line voltage waveform:

$$vm(n) := Vm \cdot \sin\left[\frac{2 \cdot \pi \cdot (n+1) \cdot Tc}{T}\right]$$

Line current waveform:

$$il(n) := Ip \cdot \sin\left[\frac{2 \cdot \pi \cdot (n+1) \cdot Tc}{T}\right]$$

$i(n) := il(n)$

Diode duty cycle: $\delta D(n) := \frac{vm(n)}{Vo}$

Center of the diode conduction interval: $Tx(n) := Tc \cdot \left(n + 1 - \frac{\delta D(n)}{2}\right)$

Inductor down slope: $A(n) := \frac{vm(n) - Vo}{L}$

Number of switching cycles per half sine: $N := \frac{T}{2 \cdot Tc}$

Difference between reference and inductor current: $B(n) := i(n) - A(n) \cdot Tx(n)$

Calculate across a half cycle: $n := 0, 1 .. N - 1$

Average current: $IDav := \frac{2}{T} \cdot \left[\sum_n \left[\frac{A(n)}{2} \cdot Tc^2 \cdot \delta D(n) \cdot (2 \cdot n + 2 - \delta D(n)) + B(n) \cdot Tc \cdot \delta D(n) \right] \right]$

$IDav = 12.079$

Define: $C(n) := \frac{A(n)^2}{3} \cdot Tc^3 \cdot \delta D(n) \cdot \left[3 \cdot (n \cdot (n + 2 - \delta D(n)) + 1 - \delta D(n)) + \delta D(n)^2 \right]$

$D(n) := A(n) \cdot B(n) \cdot Tc^2 \cdot (\delta D(n) \cdot (2 \cdot n + 2 - \delta D(n))) + B(n)^2 \cdot Tc \cdot \delta D(n)$

RMS current: $IDrms := \sqrt{\frac{2}{T} \cdot \sum_n (C(n) + D(n))}$

$IDrms = 19.215$

The following values are extracted from diode sub-section of the APT5012JNU2 datasheet

Maximum forward voltage: $Vf := 1.5$

Dynamic forward resistance: $Rd := 0.011$

Conduction losses: $Pcond := Vf \cdot IDav + Rd \cdot IDrms^2$

$Pcond = 22.18$

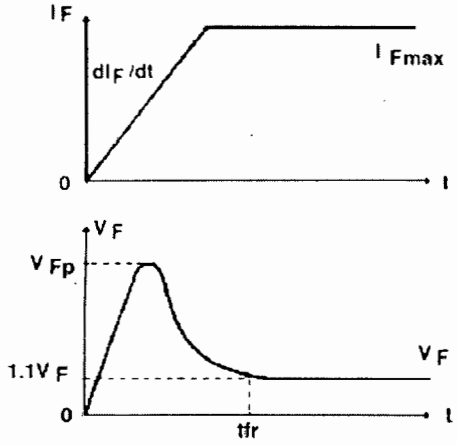
The turn-on losses are much lower than the conduction losses.The following data is extracted form the APT5012JNU2 performance graphs.

Forward recovery time: $tfr := 200 \cdot 10^{-9}$

Peak forward voltage: $Vfp := 4$

$If := IDrms$

In continuous conduction mode, the dynamic resistance and threshold voltage is required.



$$Pon := 0.4 \cdot (Vfp - Vf) \cdot If \cdot tfr \cdot Fc$$

Turn-on loss: $Pon = 0.384$

To continue calculations, a di/dt must be selected. It can be shown that there is an optimum di/dt where the efficiency of the converter is maximised.

Assuming: $diFdt := 200 \cdot 10^6$

Maximum reverse recovery current: $Irm := 15$

Softness factor: $S := 0.6$

Turn-off loss: $$Poff := \frac{1}{T} \cdot \sum_n \frac{Vo \cdot Irm^2 \cdot S}{3 \cdot diFdt}$$ $Poff = 4.275$

The above loss is far from accurate as the datasheet for the APT5012JNU2 contains very little information with regard to a softness factor and reverse recovery current at various operating points. The worst case values are assumed throughout the switching cycle.

A similar dilemma exists for the following calculation.

$$M := \frac{Irm^2 \cdot (3 + S)}{6 \cdot diFdt}$$

$$G(n) := \frac{i(n) \cdot Irm \cdot (2 + S)}{2 \cdot diFdt}$$

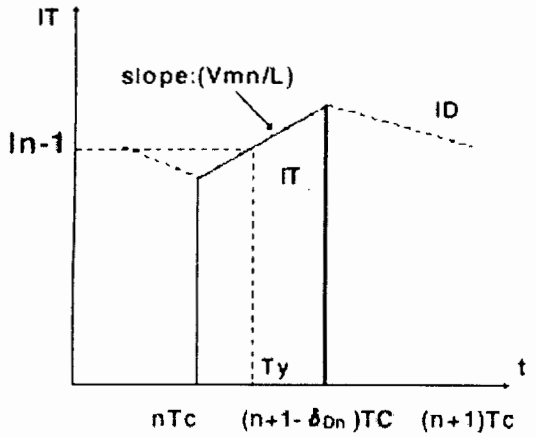
Turn-on loss in the MOSFET due to the diode: $$Pton := 2 \cdot \frac{Vo}{T} \cdot \sum_n (M + G(n))$$

$Pton = 110.562$

Total loss due to the diode: $Pdiode := Pcond + Pon + Poff + Pton$

$Pdiode = 137.401$

MOSFET power losses



Inductor slope: $A(n) := \frac{vm(n)}{L}$

Centre of the MOSFET conduction interval:

$$Ty(n) := \frac{Tc \cdot (2 \cdot n + 1 - \delta D(n))}{2}$$

Current reference: $I(n) := \frac{A(n)^2}{3} \cdot Tc^3 \cdot \left[(n + 1 - \delta D(n))^3 - n^3 \right]$

$$B(n) := Ip \cdot \sin\left(\frac{2 \cdot \pi \cdot n \cdot Tc}{T} \right) - A(n) \cdot \left(\frac{2 \cdot n + 1 - \delta D(n)}{2} \right) \cdot Tc$$

$$J(n) := \left[A(n) \cdot B(n) \cdot Tc^2 \cdot \left[(n + 1 - \delta D(n))^2 - n^2 \right] \right] + B(n)^2 \cdot Tc \cdot (1 - \delta D(n))$$

RMS current: $IMrms := \sqrt{\frac{2}{T} \cdot \sum_n (I(n) + J(n))}$ IMrms = 16.703

Conduction loss: rds := 0.12

$Pcond := rds \cdot IMrms^2$

Pcond = 33.48

$$K(n) := \frac{(I(n) + Irm)^2}{2} + \left[S \cdot \frac{Irm^2}{3} \right] + S \cdot \frac{Irm \cdot I(n)}{2}$$

Turn-on loss: $Pon := \frac{2 \cdot Vo}{T} \cdot \sum_n \left(\frac{K(n)}{diFdt} \right)$ Pon = 133.6

Total loss due to the MOSFET: $Pmosfet := Pcond + Pon$

Pmosfet = 167.08

Total losses

$$Ploss := Pdiode + Pmosfet$$

$$Ploss = 304.482 \quad \text{Watts}$$

The above result is worst case. During the calculation, assumptions were made due to the lack of information in the APT5012JNU2 datasheet. The result does however compare favourably witl other results reported in the literature.

Appendix K : Photographic images of the final converter

In section 1.5, it was stated that the thermal design is not robust. This was demonstrated when work continued on the system in Pretoria. A two-thousand metre increase in altitude from Cape Town to Pretoria rendered the original heatsink unusable. The system was then reassembled onto a 0.052°C/W forced-air cooled heatsink.

The following images were captured using a hand-held Casio QV-11 CCD camera. Later the data was transferred to the PC through an RS232 connection.

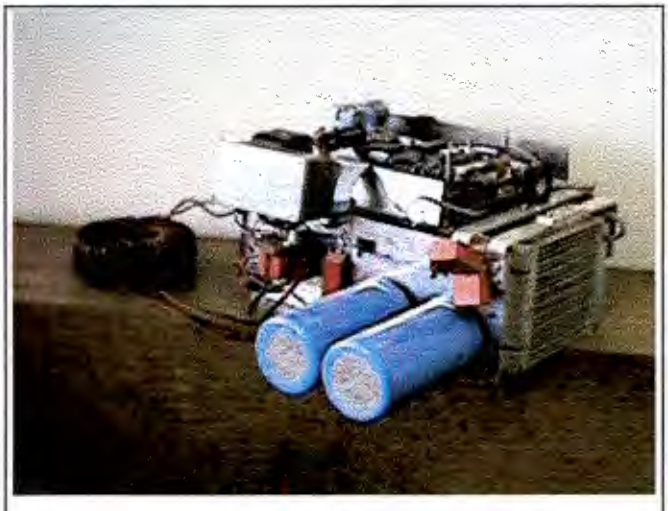


Figure 2: Power factor corrector

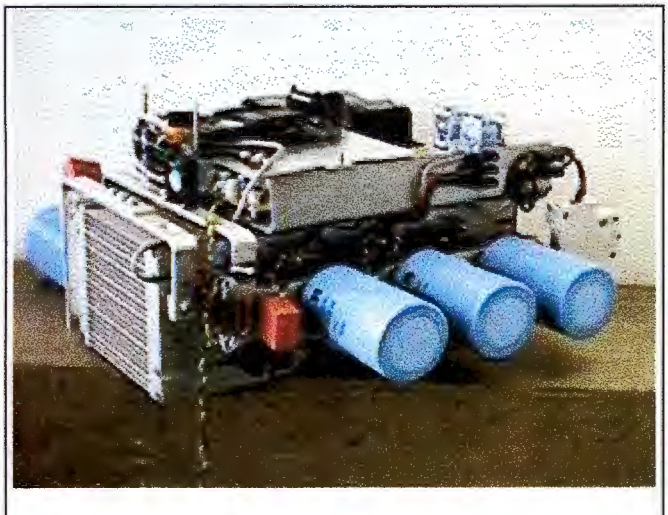


Figure 3: IGBT inverter

The placement of the DC bus capacitors virtual on top of the IGBT modules helped minimise the inductance and therefore voltage overshoot. The high speed MKS-FKP polypropylene decoupling capacitors were bolted under the electrolytic capacitors.

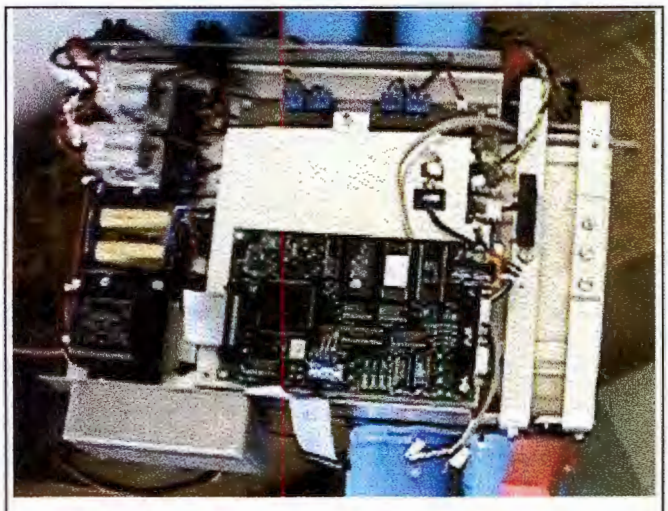


Figure 4: UPS control electronics

During the development process, a lapse in concentration resulted in the application of 15V to the 80C552 microcontroller board. As the damage was extensive a substitute board was fastened to the aluminium plate as illustrated above.

Also illustrated on the lower left of Figure 4 is the metal box used to shield the power factor controller electronics.

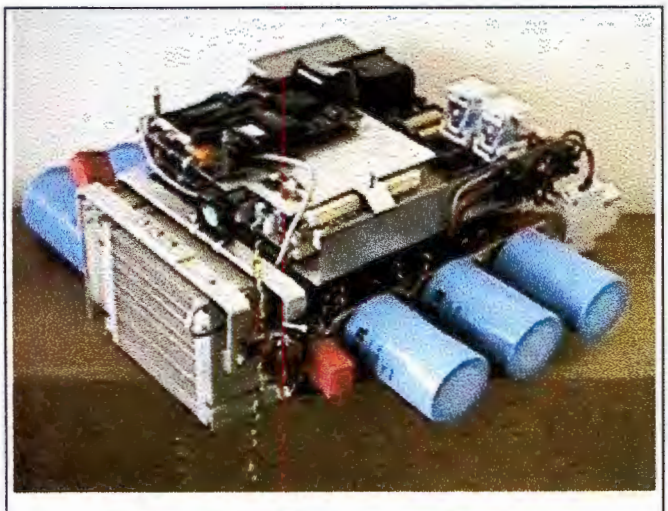


Figure 5: PFC - inverter bus bars

Aluminium bus-bars were used to connected the PFC and inverter. A miniature fan salvaged from a 486DX CPU, strapped onto the bus-bars, cooled the +5V and +15V regulators situated beneath the aluminium EMI shield.

Appendix L: System efficiency

Test 1

Vin	Iin	Vbus	Vout	Iout	Pin	Pout	%eff
150	2.67	385.60	229.00	0.99	400.50	226.71	56.61
160	2.53	385.50	229.00	0.99	404.80	226.71	56.01
170	2.38	385.40	229.00	0.99	404.60	226.94	56.09
180	2.25	385.20	229.00	1.00	405.00	228.54	56.43
190	2.15	385.10	229.00	1.00	408.50	229.00	56.06
200	2.05	385.00	229.00	1.00	410.00	229.00	55.85
210	1.96	384.70	228.00	0.98	411.60	222.30	54.01
220	1.87	384.50	229.00	0.97	411.40	222.13	53.99
230	1.81	384.30	229.00	0.96	416.30	218.70	52.53
240	1.75	384.10	228.00	0.95	420.00	216.60	51.57
250	1.68	383.90	228.40	0.95	420.00	216.98	51.66

Test 2

Vin	Iin	Vbus	Vout	Iout	Pin	Pout	%eff
150	3.34	385.20	228.00	1.33	501.00	303.24	60.53
160	3.12	385.10	228.00	1.33	499.20	303.24	60.75
170	2.92	384.90	228.00	1.33	496.40	303.24	61.09
180	2.78	384.80	228.00	1.33	500.40	303.24	60.60
190	2.63	384.60	228.00	1.33	499.70	303.24	60.68
200	2.51	384.50	228.00	1.33	502.00	303.24	60.41
210	2.41	384.40	228.00	1.33	506.10	303.24	59.92
220	2.30	384.10	228.00	1.33	506.00	303.24	59.93
230	2.22	383.90	228.00	1.33	510.60	303.24	59.39
240	2.12	383.70	228.00	1.33	508.80	303.24	59.60
250	2.06	383.50	228.00	1.33	515.00	303.24	58.88

Test 3

Vin	Iin	Vbus	Vout	Iout	Pin	Pout	%eff
150	5.47	384.20	228.00	2.63	820.50	599.64	73.08
160	5.14	384.00	228.00	2.65	822.40	604.20	73.47
170	4.78	383.80	228.00	2.65	812.60	604.20	74.35
180	4.55	383.60	228.00	2.65	819.00	604.20	73.77
190	4.30	383.50	228.00	2.65	817.00	604.20	73.95
200	4.11	383.40	228.00	2.65	822.00	604.20	73.50
210	3.91	383.20	228.00	2.65	821.10	604.20	73.58
220	3.74	383.00	228.00	2.65	822.80	604.20	73.43
230	3.58	382.70	228.00	2.65	823.40	604.20	73.38
240	3.43	382.50	228.00	2.65	823.20	604.20	73.40
250	3.30	382.30	228.00	2.65	825.00	604.20	73.24

Test 4

Vin	Iin	Vbus	Vout	Iout	Pin	Pout	%eff
150	10.08	381.40	230.30	5.30	1512.00	1220.59	80.73
160	9.33	381.40	230.10	5.26	1492.80	1210.33	81.08
170	8.82	381.30	231.00	5.26	1499.40	1215.06	81.04
180	8.32	381.20	231.00	5.26	1497.60	1215.06	81.13

190	7.80	380.90	231.00	5.26	1482.00	1215.06	81.99
200	7.42	380.70	231.00	5.26	1484.00	1215.06	81.88
210	7.08	380.60	231.00	5.26	1486.80	1215.06	81.72
220	6.76	380.30	231.00	5.26	1487.20	1215.06	81.70
230	6.49	380.20	231.00	5.26	1492.70	1215.06	81.40
240	6.21	380.00	231.00	5.26	1490.40	1215.06	81.53
250	5.97	379.70	231.00	5.26	1492.50	1215.06	81.41

Test 5

Vin	Iin	Vbus	Vout	Iout	Pin	Pout	%eff
180	10.15	379.50	225.00	6.84	1827.00	1539.00	84.24
190	9.95	379.30	229.70	6.93	1890.50	1591.82	84.20
200	9.44	379.20	229.70	6.93	1888.00	1591.82	84.31
210	9.10	379.00	228.00	6.98	1911.00	1591.44	83.28
220	8.66	378.70	229.00	6.95	1905.20	1591.55	83.54
230	8.17	378.60	229.00	6.91	1879.10	1582.39	84.21
240	7.88	378.50	229.00	6.91	1891.20	1582.39	83.67
250	7.53	378.10	228.00	6.94	1882.50	1582.32	84.05

Test 6

Vin	Iin	Vbus	Vout	Iout	Pin	Pout	%eff
180	14.06	376.20	230.00	9.56	2530.80	2198.80	86.88
190	13.60	376.20	228.00	9.46	2584.00	2156.88	83.47
200	12.60	376.10	229.00	9.56	2520.00	2189.24	86.87
210	12.20	376.20	230.00	9.42	2562.00	2166.60	84.57
220	11.55	376.00	229.00	9.58	2541.00	2193.82	86.34
230	11.00	375.50	230.00	9.53	2530.00	2191.90	86.64
240	10.52	375.50	228.00	9.59	2524.80	2186.52	86.60
250	10.12	375.50	228.00	9.44	2530.00	2152.32	85.07

Test 7

Vin	Iin	Vbus	Vout	Iout	Pin	Pout	%eff
180	18.60	372.00	227.00	12.00	3348.00	2724.00	81.36
190	16.75	372.60	227.00	12.01	3182.50	2726.27	85.66
200	16.01	372.50	230.00	12.06	3202.00	2773.80	86.63
210	15.35	372.30	229.00	12.12	3223.50	2775.48	86.10
220	14.65	372.50	228.00	12.11	3223.00	2761.08	85.67
230	14.14	372.40	228.00	12.08	3252.20	2754.24	84.69
240	13.07	372.40	229.00	12.06	3136.80	2761.74	88.04
250	12.60	372.40	230.00	12.08	3150.00	2778.40	88.20